

Real Time Clock Module

JR8130-32-I2C-UB-T(-40/+85)-LF

Jauch Revision History

Rev. No.	Date	Page	Description
01	2026/10/01	All	First released

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Build-in backup battery charge control function
SERIAL-INTERFACE REAL TIME CLOCK MODULE

JR8130

- Built in frequency adjusted 32.768 kHz crystal unit.
- Interface type: I²C-Bus interface (up to 400 kHz)
- Wide operating voltage range: 1.6Vto5.5V
- Wide timekeeper voltage range: 1.1Vto5.5V
- Auto power switching function: Switchover by main power supply monitor.
- Backup battery charge control function: For rechargeable lithium batteries.
- Low leak current: Leak current from a backup power supply pin. 5 nA Max.
- Reset function: At low supply voltage, external reset signal is generated.
- Low voltage detection: Supply voltage and backup voltage detection
- Time correction: Digital offset function
- Various functions including full calendar, alarm, timer, etc.

1. Overview

JR8130 is a real-time clock module with the I²C serial interface. A 32.768 kHz crystal and oscillator is built-in it. The real-time clock function incorporates not only a calendar and clock counter for the year, month, day, day of the week, hour, minute, and second, but also a time alarm, wakeup timer, time update interruption and multiple other features. By the backup battery charge control function and the interface power supply input pin, JR8130 can support various power supply configurations.

All these useful functions are implemented in a thin, compact ceramic package, which makes it suitable for various kinds of small electronic devices, low power IoT devices etc.

2. Block Diagram

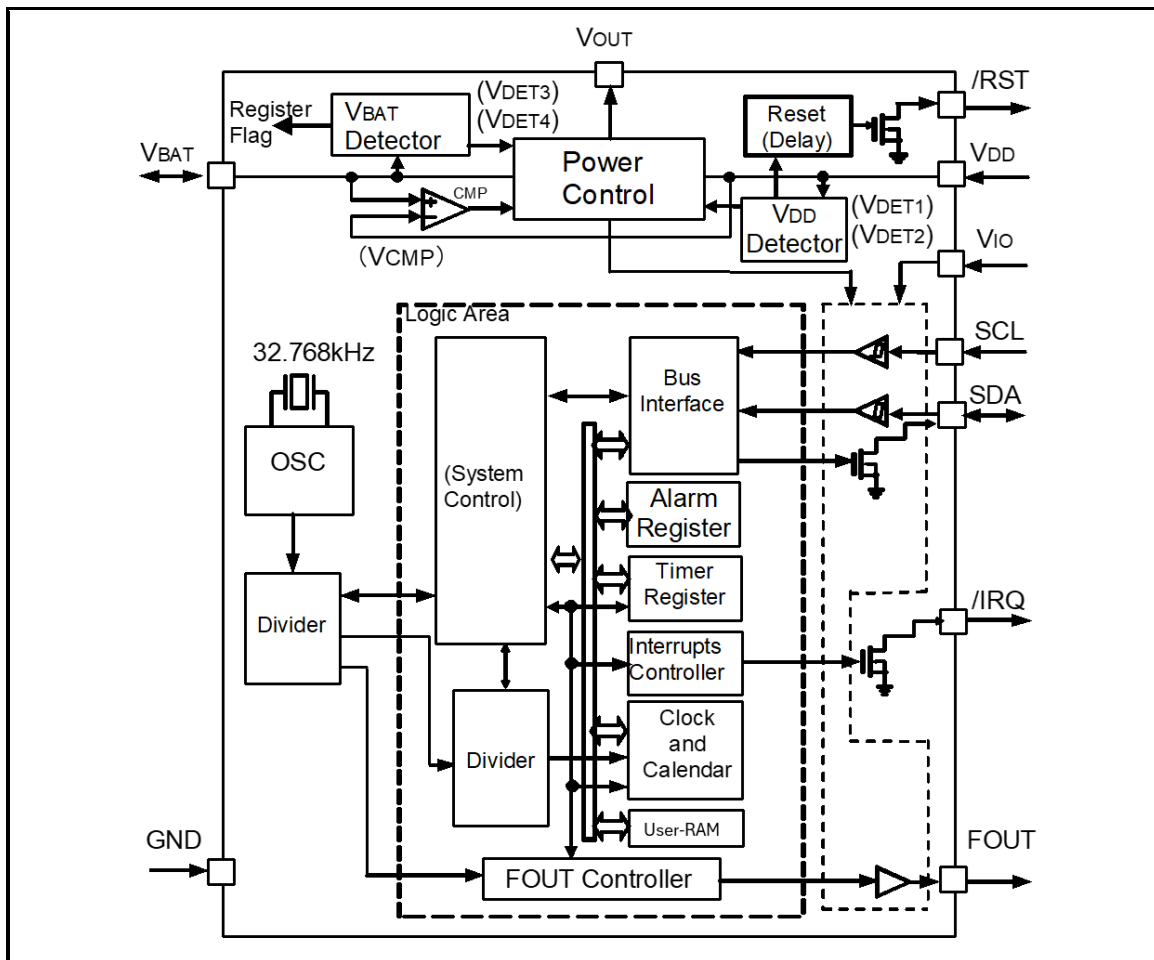


Figure 1 Block Diagram

3. Terminal description

3.1. Terminal connections

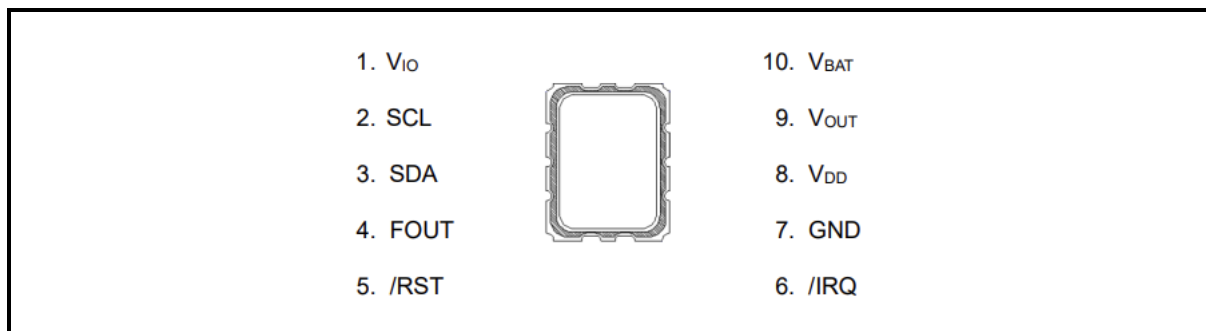


Figure 2 Package

3.2. Pin Functions

Signal name	I/O	Function
SCL	Input	Serial clock input pin.
SDA	Bi-directional	Data input and output pin.
FOUT	Output	Frequency output pin with output control function. (CMOS) Output frequency can be disabled or selected as 32.768 k Hz, 1024 Hz, 1 Hz output.
/ RST	Output	In case of V _{DD} voltage drop detection, a reset signal is outputted. (N-ch open drain). In case of V _{DD} voltage rise detection, it releases the reset signal after 60ms. This pin is also operational in the backup mode.
/ IRQ	Output	Interrupt output by Alarm and Timer events (N-ch open drain) This pin is also operational in the backup mode.
V _{DD}	–	This is a power-supply pin for the internal logic functions.
V _{IO}	–	This is an interface power supply pin. Connect the same power supply as the MCU.
V _{OUT}	–	Internal voltage output pin. Connect smoothing capacitor of 1.0uF
V _{BAT}	–	This is a power supply pin for backup battery. Use this pin to connect a large-capacity capacitor, a secondary battery, and a primary battery. In a backup mode, the voltage is supplied inside by this pin.
GND	–	Connected to ground.

Table 1 Pin Description

Note: Connect a bypass capacitor of 0.1μF or more between power supply pins and GND pin.

Note: Input pins can accept input levels up to 5.5V regardless of V_{IO} applied voltage.

Note: Open drain pins are able to Pull-up to 5.5V regardless of V_{IO} applied voltage.

Note: Keep the FOUT, /RST, /IRQ terminals unconnected when not in use. Don't connected to GND or V_{DD}

4. Examples of external connection

4.1. Examples of power supply connection

When using a secondary battery (INIEN bit = 1, CHGEN bit = 1)
 When V_{DD} is less than or equal to V_{DET1} , the / RST output is asserted to Low regardless of the V_{IO} voltage.
 At the same time, the I²C interface and FOUT output are disabled.
 When V_{DD} drops below $-V_{DET2}$, the RTC power supply is switched from V_{DD} to V_{BAT} .

In case of common power source of V_{DD} and V_{IO} .

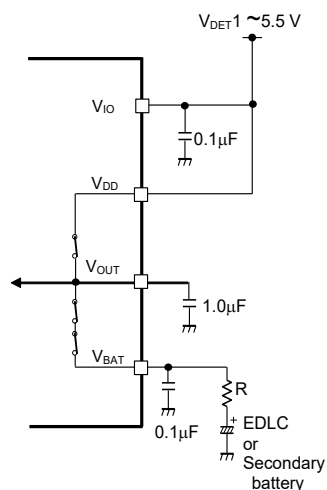


Figure 3 Circuit example 1

In case of a separated power source.

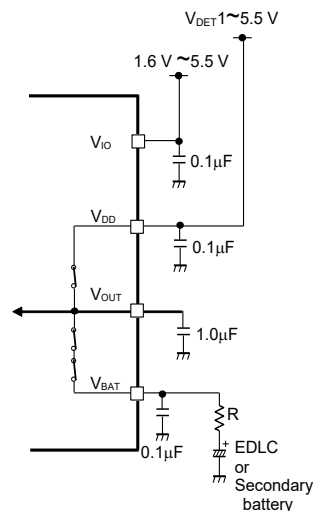


Figure 4 Circuit example 2

When using primary battery (INIEN bit = 1, CHGEN bit = 0)
 When V_{DD} is less than or equal to V_{DET1} , the / RST output is asserted to Low regardless of the V_{IO} voltage.
 At the same time, the I²C interface and FOUT output are disabled.
 When V_{DD} drops below $-V_{DET2}$, the RTC power supply is switched from V_{DD} to V_{BAT} .

In case of common power source of V_{DD} and V_{IO} .

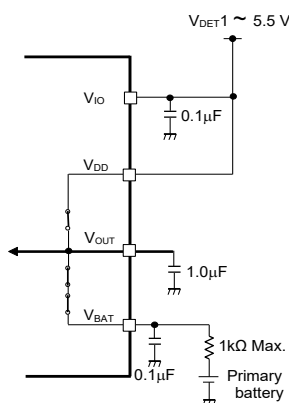


Figure 5 Circuit example 3

In case of a separated power source.

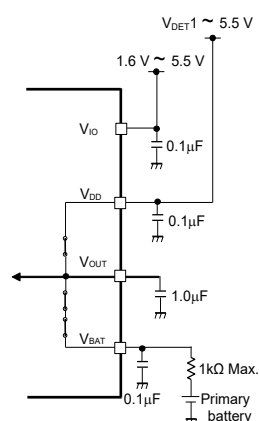
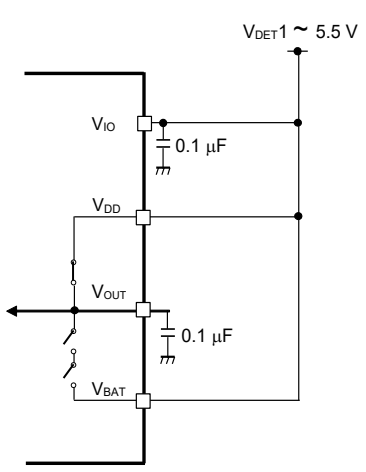
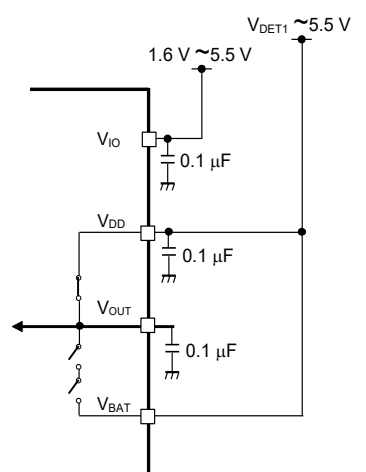
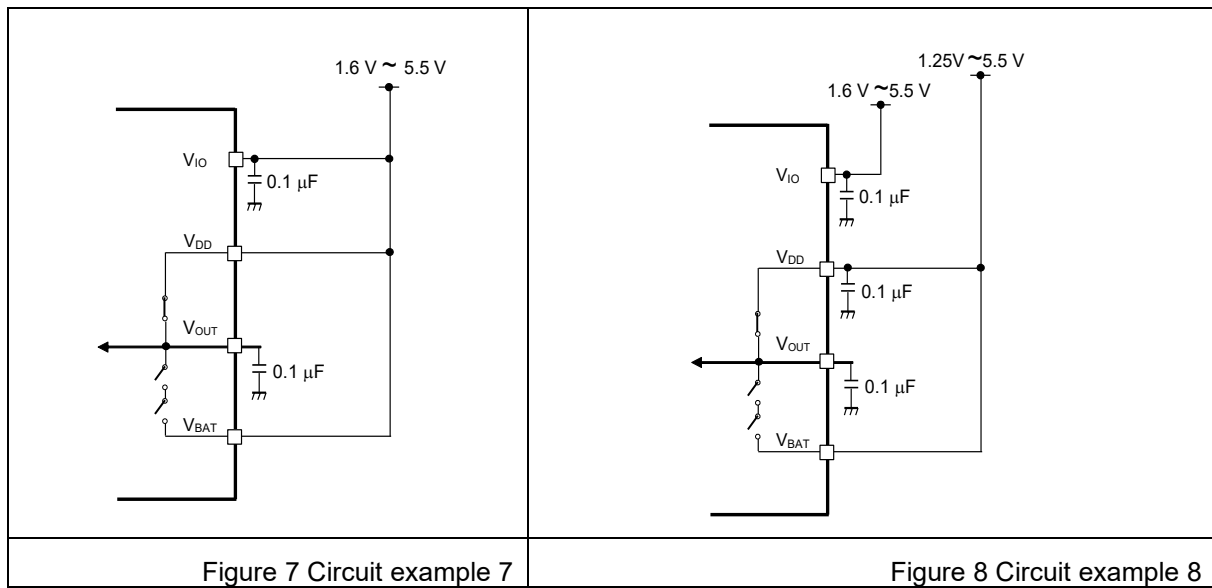


Figure 6 Circuit example 4

4.2. Example of connection circuit that does not use the power switching function

A case of not using the power switching function. (INIEN bit = 1, CHGEN bit = 0) Power is always supplied from V_{DD}, but for stable operation, connect V_{BAT} to V_{DD} rather than let it open. When V_{DD} is V_{DET1} or less, the /RST output is asserted to Low regardless of the V_{IO} voltage, and the I²C interface and FOUT output are disabled.	
When the I ² C-Bus and V_{DD} are the same power source, please use I ² C with more than V_{DET1} . RTC data is updated at 1.1 V minimum.	When the I ² C voltage and V_{DD} voltage are different, please use V_{DD} more than V_{DET1} and V_{IO} more than 1.6V.
In case of common power source of V_{DD} and V_{IO} .	In case of a separated power source.
	
Figure 7 Circuit example 5	Figure 8 Circuit example 6

A case of not using the power switching function. (INIEN bit = 0, CHGEN bit = 0) When V_{DD} is less than V_{DET1} and the RTC is used with INIEN = 0 of after power-on reset, power is always supplied from V_{DD}. For stable operation, do not open V_{BAT} but connect it to V_{DD}.	
When the I ² C-Bus and V_{DD} are the same power source, please use I ² C at more than 1.6V. I ² C is not disabled even if V_{DD} is below V_{DET1} voltage. RTC data is updated at 1.1 V minimum.	When the I ² C voltage and V_{DD} voltage are different, please use V_{DD} more than V_{DET1} and V_{IO} more than 1.6V. I ² C is not disabled even if V_{DD} is below V_{DET1} voltage. RTC data is updated at 1.1 V minimum.
In case of common power source of V_{DD} and V_{IO} .	In case of the separated power source.



For details on the timing of power supply and register access, refer to "[10. I²C interface timing](#)", when power is turned on / off. Please install each bypass capacitor as close as possible to V_{DD} , V_{BAT} , V_{IO} , V_{OUT} .

5. External Dimensions / Marking Layout

5.1. External Dimensions

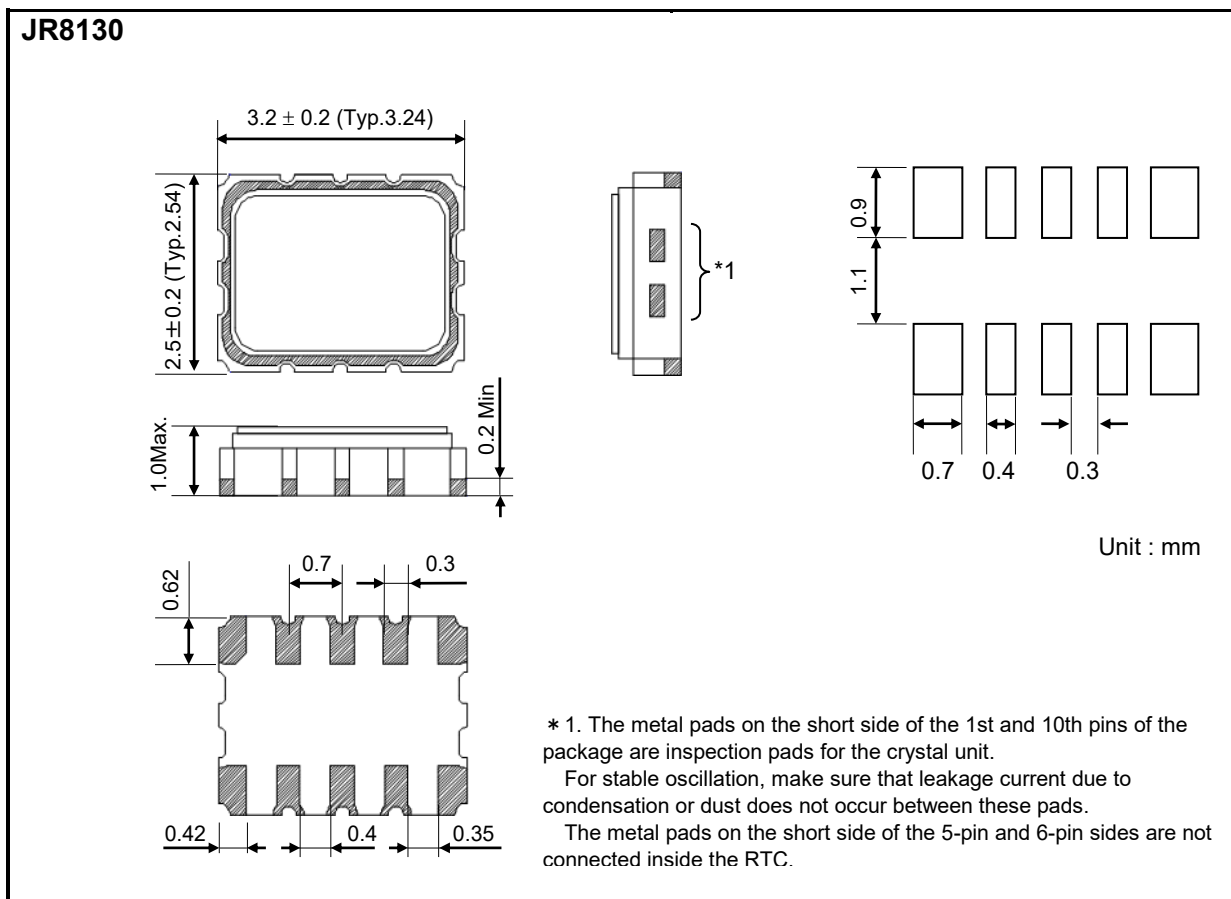


Figure 9 External Dimension and Soldering pattern

5.2. Marking Layout

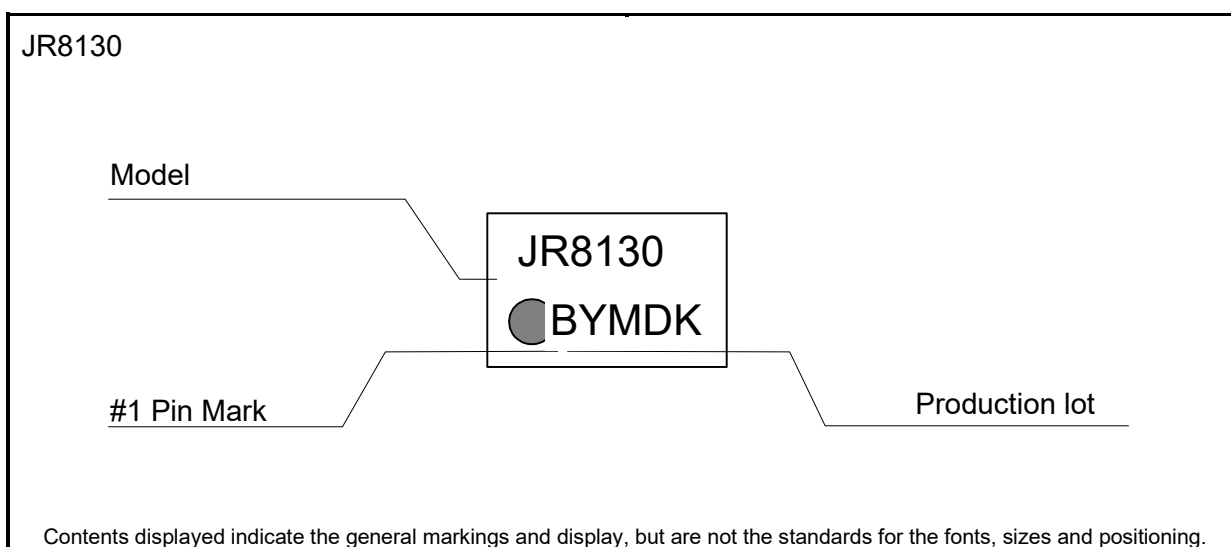


Figure 10 Marking Layout

6. Absolute Maximum Ratings

Item	Symbol	Condition	Rating	Unit
Supply voltage	V _{DD}	–	–0.3 ~ +6.5	V
Internal voltage	V _{OUT}	–	–0.3 ~ +6.5	V
Backup supply voltage	V _{BAT}	–	–0.3 ~ +6.5	V
Interface supply voltage	V _{IO}	–	–0.3 ~ +6.5	V
Input voltage 1	V _{IN1}	SCL, SDA	–0.3 ~ +6.5	V
Output voltage 1	V _{OUT1}	/RST, /IRQ, SDA	–0.3 ~ +6.5	V
Output voltage 2	V _{OUT2}	FOUT	–0.3 ~ V _{IO} +0.3	V
		When stored separately, without packaging	–55 ~ +125	°C

Table 2 Absolute Maximum Rating

7. Recommended Operating Conditions

Unless otherwise specified, GND=0V, Ta=-40°C to +85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating supply voltage	V _{DD}	INIEN = 0	1.25	3.0	5.5	V
		INIEN = 1	V _{DET1}	3.0	5.5	V
Interface supply voltage	V _{IO}	INIEN=0	1.6	3.0	5.5	V
		INIEN=1 V _{DD} > V _{DET1}				
Clock supply voltage	V _{CLK}	Backup operation mode (V _{OUT})	1.1	3.0	5.5	V
Operating temperature	T _{use}	No condensation	-40	+25	+85	°C

Minimum clock supply voltage of V_{CLK} is available after initializing in V_{DD}>V_{DET1}.

Table 3 Recommended Operation Condition

8. Frequency Characteristics Operating supply voltage

Unless otherwise specified, GND=0V, Ta=-40°C to +85°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Output frequency	fo		32.768 (Typ.)			kHz
Frequency stability	$\Delta f/f$	Ta=+25°C V _{DD} =3.0V	5 ±23 (*1)			×10 ⁻⁶
Frequency/voltage characteristics	f/V	Ta=+25°C V _{DD} =1.1V~5.5V	-2		+2	×10 ⁻⁶ /V
Frequency/temperature characteristics	T _{0p}	Ta=-20°C~+70°C V _{DD} =3.0V; +25°C reference	-120		+10	×10 ⁻⁶
Oscillation start time	t _{str}	V _{DD} =2.75V~5.5V Internal crystal oscillation starts		0.19	1.0	s
Aging	fa	Ta=+25°C, V _{BAT} =3.0V; first year	-5		+5	×10 ⁻⁶ /year

*1) The monthly error is equal to ±60 s Max. (excluding offset)

Table 4 Frequency Characteristics

9. Electrical Characteristics

9.1. DC characteristics

Unless otherwise specified, GND=0V, $V_{BAT} = V_{DD} = 1.1 \text{ V} \sim 5.5 \text{ V}$, $V_{IO} = 1.6 \text{ V} \sim 5.5 \text{ V}$ $T_a = -40^\circ\text{C}$ to $+85^\circ\text{C}$

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Current consumption in normal operation mode without FOUT (1)	I_{DD}	SCL = SDA = "H", FOUT = OFF, /IRQ = OFF, $V_{DD}=V_{IO} = 3.0 \text{ V}$, $-40^\circ\text{C} \sim +85^\circ\text{C}$ CHGEN = 0b or $V_{BAT} \geq V_{DET3}$		1500	1600	nA
Current consumption in normal operation with FOUT (2)	I_{32k}	SCL = SDA = "H", FOUT = 32.768 kHz, /IRQ = OFF, $V_{DD}=V_{IO} = 3.0 \text{ V}$, $-40^\circ\text{C} \sim +85^\circ\text{C}$ FOUT pin CL = 15 pF CHGEN = 0b or $V_{BAT} \geq V_{DET3}$		3.5	4.0	μA
Current consumption in backup mode(3)	I_{BAT}	SCL = SDA = "L", $V_{BAT} = 3.0 \text{ V}$, $V_{DD}=V_{IO} = 0.0 \text{ V}$, $-40^\circ\text{C} \sim +85^\circ\text{C}$		300	500	nA
Detector Threshold Voltage1 (rising edge of V_{DD})	$+V_{DET11}$	2.75 V setting Reset-releases	2.72	2.80	2.88	V
Detector Threshold Voltage1 (falling edge of V_{DD})	$-V_{DET11}$	2.75 V setting Reset output	2.67	2.75	2.83	V
Detector Threshold Voltage2 (rising edge of V_{DD})	$+V_{DET12}$	2.7 V setting Reset-releases	2.67	2.75	2.83	V
Detector Threshold Voltage2 (falling edge of V_{DD})	$-V_{DET12}$	2.7 V setting Reset output	2.62	2.70	2.78	V
Detector Threshold Voltage3 (rising edge of V_{DD})	$+V_{DET2}$	Switching voltage from V_{BAT} to V_{DD}	1.25	1.35	1.45	V
Detector Threshold Voltage3 (falling edge of V_{DD})	$-V_{DET2}$	Switching voltage from V_{DD} to V_{BAT}	1.20	1.30	1.40	V
Detector Threshold Voltage1 (rising edge of V_{BAT})	$+V_{DET31}$	Charge stop voltage (full charge) BFVSEL=00b	2.94	3.02	3.10	V
Detector Threshold Voltage1 (falling edge of V_{BAT})	$-V_{DET31}$	Recharge voltage. BFVSEL=00b	2.89	2.97	3.05	V
Detector Threshold Voltage2 (rising edge of V_{BAT})	$+V_{DET30}$	Charge stop voltage (full charge) BFVSEL=10b	2.84	2.92	3.00	V
Detector Threshold Voltage2 (falling edge of V_{BAT})	$-V_{DET30}$	Recharge voltage. BFVSEL=10b	2.79	2.87	2.95	V
Detector Threshold Voltage3 (rising edge of V_{BAT})	$+V_{DET32}$	Charge stop voltage (full charge) BFVSEL=01b	3.00	3.08	3.16	V
Detector Threshold Voltage3 (falling edge of V_{BAT})	$-V_{DET32}$	Recharge voltage. BFVSEL=01b	2.95	3.03	3.11	V
V_{BAT} end voltage	$-V_{DET4}$	Low V_{BAT} detection Register flag VBLF = 1b	2.32	2.40	2.48	V
$V_{DD}-V_{OUT}$ off-leak current	ISW1	$V_{OUT}=3.0 \text{ V}$ $V_{DD}=0.0 \text{ V}$			5.0	nA
$V_{BAT}-V_{OUT}$ off-leak current	ISW2	$V_{BAT}=3.0 \text{ V}$ $V_{OUT}=0.0 \text{ V}$			5.0	nA

Table 5 DC characteristics(1)

Unless otherwise specified GND=0V $V_{BAT} = V_{DD} = 1.1V \sim 5.5V$ $V_{IO} = 1.6V \sim 5.5V$ $T_a = -40^{\circ}C \sim +85^{\circ}C$

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
V _{OUT} output voltage 1	V _{VOUT1}	V _{DD} = 3.0 V I _{OUT} = 1 mA			V _{DD} -0.06		V
V _{OUT} output voltage 2	V _{VOUT2}	V _{BAT} = 3.0 V I _{OUT} = 0.1 mA			V _{BAT} -0.02		V
High-level input voltage	V _{IH1}	SCL, SDA		0.8 × V _{IO}		5.5	V
Low-level input voltage	V _{IL}	SCL, SDA		GND – 0.3		0.2 × V _{IO}	V
High-level output voltage	V _{OH}	FOUT	I _{OH} = -1 mA	V _{IO} -0.5		V _{IO}	V
Low-level output voltage	V _{OL1}	FOUT	I _{OL} = 1 mA	GND		GND+0.5	V
	V _{OL2}	/RST,/IRQ	V _{IO} = 5 V, I _{OL} = 1 mA	GND		GND+0.25	V
	V _{OL3}		V _{IO} = 3 V, I _{OL} = 1 mA	GND		GND+0.4	V
	V _{OL4}	SDA	V _{IO} ≥ 2 V, I _{OL} = 3 mA	GND		GND+0.4	V

Table 6 DC characteristics (2)

9.2. AC characteristics

 Unless otherwise specified GND = 0 V $V_{IO} = 1.6 V \sim 5.5 V$ $T_a = -40^{\circ}C \sim +85^{\circ}C$

Item	Symbol	Standard-Mode (f _{SCL} =100 kHz)		Fast-Mode (f _{SCL} =400 kHz)		Unit
		Min.	Max.	Min.	Max.	
SCL clock frequency	f _{SCL}		100		400	kHz
Start condition setup time	t _{SU;STA}	4.7		0.6		μs
Start condition hold time	t _{HD;STA}	4.0		0.6		μs
Data setup time	t _{SU;DAT}	250		100		ns
Data hold time	t _{HD;DAT}	0		0		ns
Stop condition setup time	t _{SU;STO}	4.0		0.6		μs
Bus idle time between start condition and stop condition	t _{BUF}	4.7		1.3		μs
Time when SCL = "L"	t _{LOW}	4.7		1.3		μs
Time when SCL = "H"	t _{HIGH}	4.0		0.6		μs
Rise time for SCL and SDA	t _r		1.0		0.3	μs
Fall time for SCL and SDA	t _f		0.3		0.3	μs
Allowable spike time on bus	t _{SP}		50		50	ns

Table 7 AC characteristics

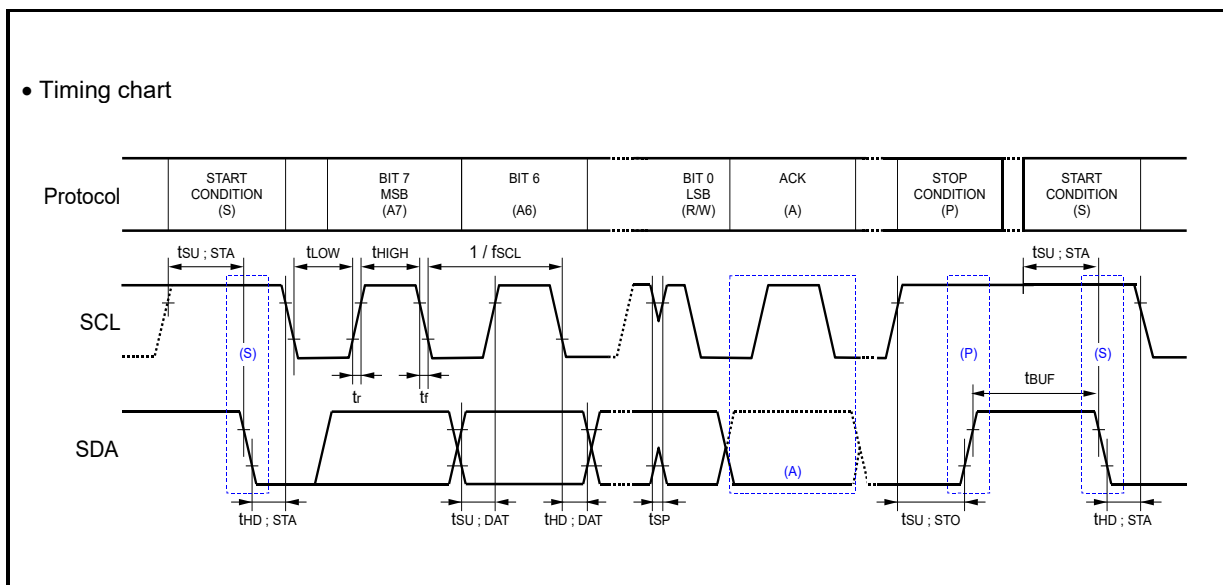


Figure 11 I²C-Bus Interface Timing Chart

Warning: When accessing this device, the entire communication sequence – from issuing the start condition to transmitting the stop condition – must be completed within 0.95 seconds. If such communication requires 0.95 seconds or longer, the I²C-Bus interface will be reset by the internal bus timeout function.

When bus-time-out occurs, SDA turns to Hi-Z input mode.

Note: During access to the time registers, the time counting is on hold. This means that up to 1 second can be “lost” in case of unsuccessful communication as mentioned above. Ensure that an I²C start condition is issued before transmitting the RTC’s slave address; otherwise, the address would be interpreted as shifted by one bit.

※Unless otherwise specified GND = 0 V , $V_{IO} = 1.6 \text{ V} \sim 5.5 \text{ V}$, $T_a = -40 \text{ }^{\circ}\text{C} \sim +85 \text{ }^{\circ}\text{C}$

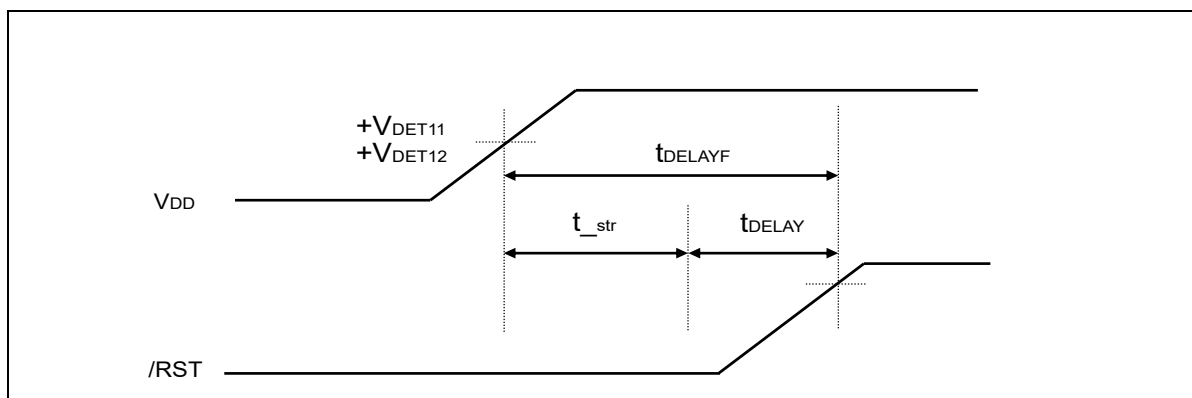
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
FOUT symmetry	SYM	50% V_{IO} Level	40		60	%

Table 8 AC characteristics (FOUT)

9.3. AC characteristics (3)

Item	Symbol	Min.	Typ.	Max.	unit
Reset internal delay time	t_{DELAY}		60		ms
Reset delay time (Initial power ON)	t_{DELAY_F}		250 ($t_{str} + t_{DELAY}$)		ms

Table 9 AC Characteristics (Reset)

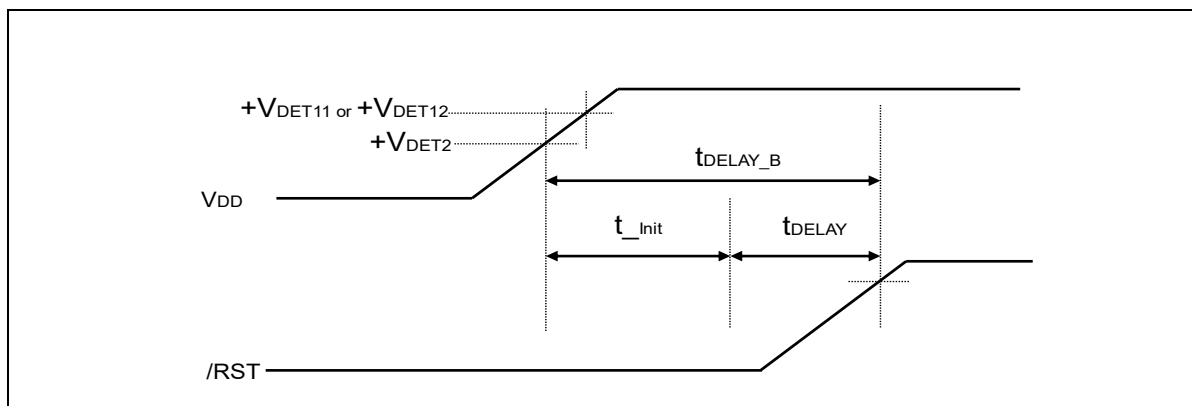


* t_{str} is oscillation startup time. Typical value is 190ms. See "Table4".

Figure 12 Reset signal timing chart (Power initial supply)

Item	Symbol	Min.	Typ.	Max.	unit
Voltage detection time to reset release.	t_{int}			35	ms
Reset delay time (Recovery from Backup) $t_{int} + t_{DELAY}$	t_{DELAY_B}	60		95	ms

Table 10 Reset timing



t_{int} is an intermittent drive timing of a V_{DET2} detecting circuit. Maximum value is 35 ms.

Figure 13 Reset signal timing chart (Recovery from backup)

10. Interface timing when power is turned ON / OFF

10.1. Restrictions of I²C-Bus interface in the initial power on.

The operation of the RTC register is linked to the oscillation clock of the built-in crystal unit. Therefore, it will not operate normally when the oscillation is stopped. It is recommended that the initialization at the time of initial power-on is performed after the oscillation start time t_{str} characteristic (1sec max.) has fulfilled.

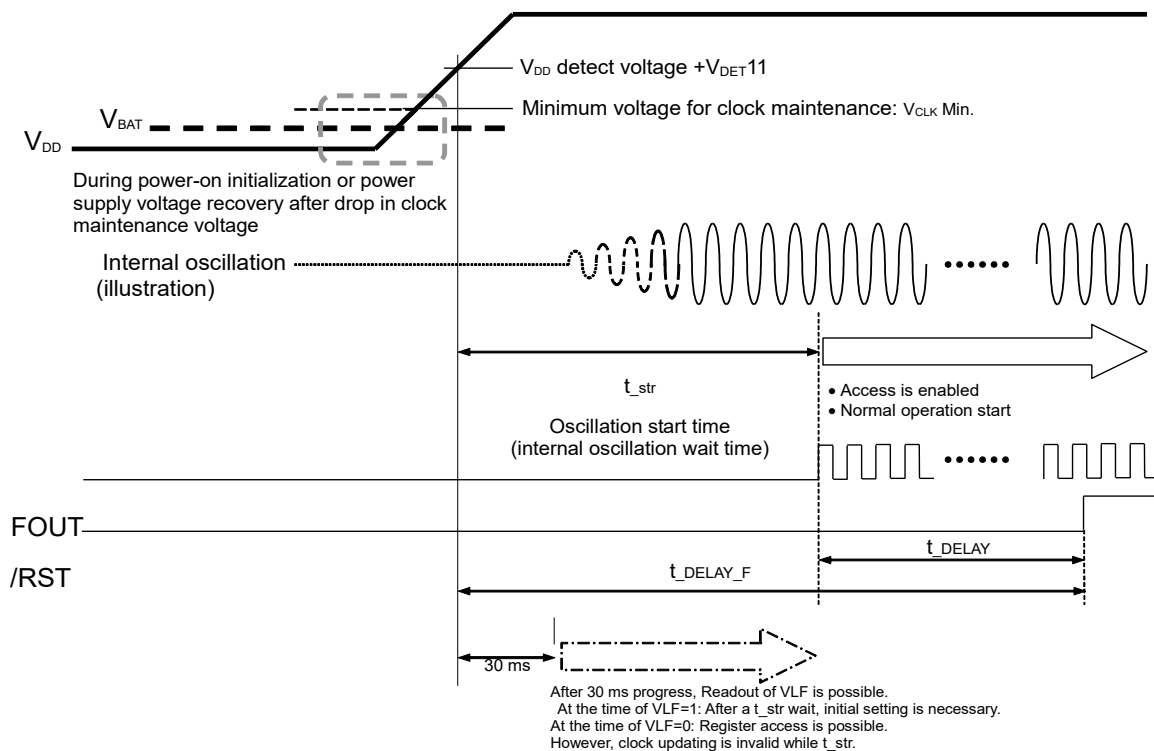


Figure 14 Power supply initial sequence

10.2. Precautions for power ON / OFF

- 1: To ensure that the power-on reset correctly at the initial power-on, both V_{DD} and V_{BAT} should be held at GND for 10 seconds or longer before V_{DD} is switched on.
- 2: Initial power-on $tR1$ is a necessary condition for enabling power-on reset. If this condition is not satisfied, power-on reset may not work. As a result, the time accuracy and current consumption may not meet the specifications. Please reset by software. See [18.2 Software Reset](#).
- 3: If the rise or fall characteristics of V_{DD} (tF or $tR2$) fall outside the specified ranges, various malfunctions may occur. These include a temporary halt of the crystal oscillation, assertion of VLF caused by V_{OUT} dropping below V_{CLK} , and other similar effects.
- 4: The enable timing of the I²C-Bus interface varies depending on whether V_{DD} is being applied for the first time or being restored from backup mode. See the t_{CL} and t_{CU} specifications in the chart below.
- 5: These specifications don't mean a noise characteristic of a power supply of RTC. Do not use the amplitude signal output from a signal generator etc., as a power source.

10.3. V_{DD} ON / OFF when using power switching (INIEN = 1)

See "4.1. Examples of power supply connection"_Circuit EX1, 2, 3.

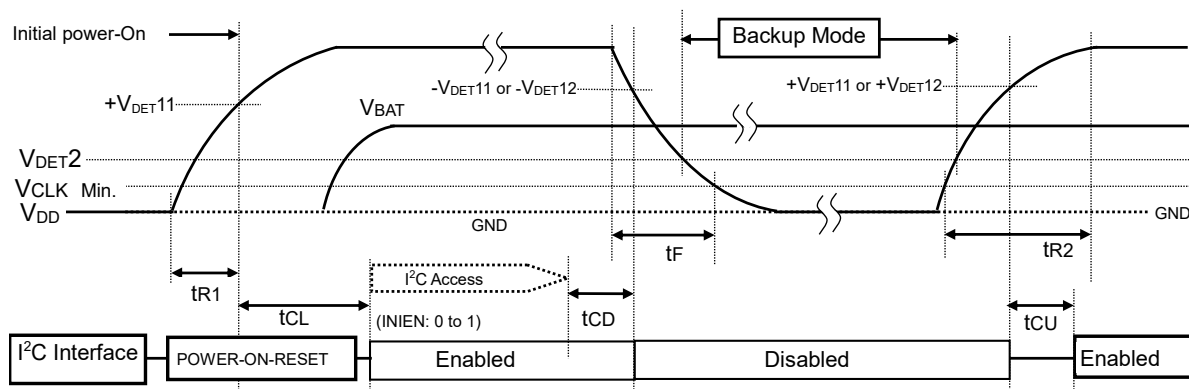


Figure 15 Power-On sequence1

10.4. V_{DD} ON / OFF when power switching is not used (INIEN = 0)

See "4.1. Examples of power supply connection"_Circuit EX4.

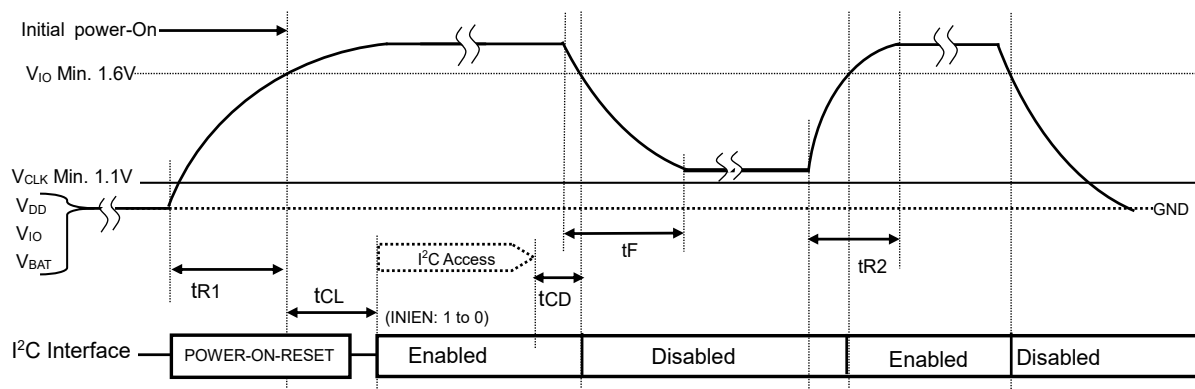


Figure 16 Power-On sequence2

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply rise time	tr1	From GND to $V_{DD} = +V_{DET11}$	0.1	-	10	ms / V
Access wait time	tCL	$V_{DD} = +V_{DET11}$ to Access start		-	-30	ms
Access suspended time	tCD	The time from the end of I2C access to the disable of I2C	0	-	-	ms
Power supply fall time	tF	From V_{DD} to $V_{DD} = V_{CLK}$	1	-	-	ms / V
Power supply rise time	tr2	Time to restore V_{DD} to operating voltage	1	-	-	ms / V
Access wait time	tCU	$V_{DD} = +V_{DET1X}$ to Access start		-	35	ms

tR1, tR2, and tF specify that there is no voltage fluctuation faster / slower than the Min / Max specifications within the specified section.

Table 11 Power supply characteristics

The risk when specifications of timing for V_{DD} and V_{BAT} were not satisfied, refer to the following.

Item	Risk of fast fluctuations	Risk of slow fluctuations
tR1	Power-On-Reset doesn't occur.	
tR2	The FOUT waveform disappears momentarily, and clock time is momentarily delayed. A data of RTC loss. A set of VLF.	None
tF		

Table 12 Risks of unsatisfying timing of V_{DD} and V_{BAT}

V_{DD} and V_{BAT} in Figures 15 and 16 are the voltages of V_{DD} and V_{BAT} pins of JR8130. Regarding access to the clock register after the initial power-on, See "10.1 restrictions of I2C interface in the initial power on".

The clock from FOUT is outputted after tCU. When status of $V_{DD} = V_{BAT} = GND$ doesn't keep more than 10seconds before initial power-on, the Power-On-Reset may not work even if the tR / tF specifications are satisfied.

10.5. Power-on order

V_{DD} and V_{IO} are separated and can give different voltage levels. In specifications range, the voltage relations (V_{DD} and V_{IO}) are free. When a voltage higher than V_{DET+} is supplied to the main power source (V_{DD}), an unstable V_{IO} level between GND and V_{DD} may cause through-current. In this condition, the resulting through-current may generate a leakage current of up to 10 μA .

If 10 μA max. is not permitted, the below power-up sequence chart would be recommended. When the power-source supply of V_{DD} is carried out earlier than V_{IO} , please start V_{IO} from a GND level and not become unstable. If this 10 μA current is acceptable, V_{DD} , V_{IO} , and V_{BAT} may be applied with independent timing without causing any issues. However, by this through-current, RTC does not get damaged and the malfunction does not occur.

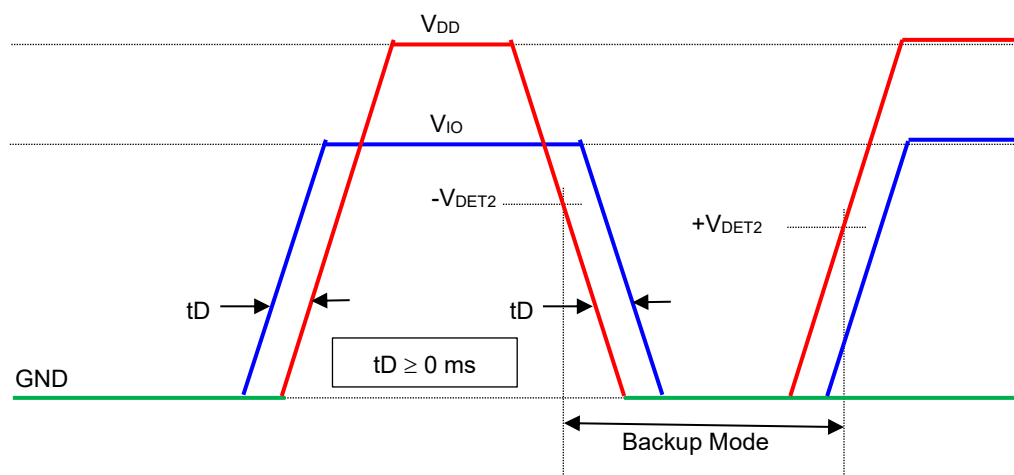
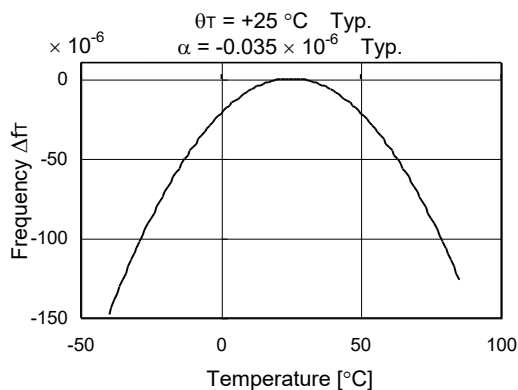


Figure 17 Power-on sequence

11. Reference Information

11.1. Reference Data

(1) Example of frequency and temperature characteristics



[Finding the frequency stability]

1. Frequency and temperature characteristics can be approximated using the following equations.

$$\Delta f_T = \alpha (\theta_T - \theta_X)^2$$

- Δf_T : Frequency deviation in any temperature
- α [$1 / ^{\circ}\text{C}^2$] : Coefficient of secondary temperature
(-0.035 ± 0.005) $\times 10^{-6} / ^{\circ}\text{C}^2$
- θ_T [$^{\circ}\text{C}$] : Ultimate temperature ($+25 \pm 5\text{ }^{\circ}\text{C}$)
- θ_X [$^{\circ}\text{C}$] : Any temperature

2. To determine overall clock accuracy, add the frequency precision and voltage characteristics.

$$\Delta f/f = \Delta f/f_0 + \Delta f_T + \Delta f_V$$

- $\Delta f/f$: Clock accuracy (stable frequency) in any temperature and voltage.
- $\Delta f/f_0$: Frequency precision
- Δf_T : Frequency deviation in any temperature.
- Δf_V : Frequency deviation in any voltage.

3. How to find the date difference

$$\text{Date Difference} = \Delta f/f \times 86400 \text{ s}$$

* For example: $\Delta f/f = 11.574 \times 10^{-6}$ is an error of approximately 1 second / day.

Figure 18 Frequency temperature characteristics

12. Application Notes

1) Notes on handling

This module uses a C-MOS IC to realize low power consumption. Carefully note the following cautions when handling.

(1) Static electricity

While this module has built-in circuitry designed to protect it against electrostatic discharge, the chip could still be damaged by a large discharge of static electricity. Containers used for packing and transport should be constructed of conductive materials. In addition, only soldering irons, measurement circuits, and other devices which do not leak high voltage should be used with this module, which should also be grounded when such devices are being used.

(2) Noise

If a signal with excessive external noise is applied to the power supply or input pins, the device may malfunction or "latch up". In order to ensure stable operation, connect a filter capacitor (preferably ceramic) of greater than 0.1 μF as close as possible to the power supply pins. Also, avoid placing any device that generates high level of electromagnetic noise near this module.

(3) Voltage levels of input pins

When the voltage of output of the input voltage specifications range input into an input terminal constantly, a penetration electric current occurs. Thus, current consumption increases very much. This causes latch-up, and there is the case that, as a result, a built-in IC is destroyed. Please use an input terminal according to input voltage specifications. Furthermore, please give the V_{IO} or GND most recent voltage as much as possible.

(4) Handling of unused pins

Disposal of unused input terminals. When an input terminal is open state, it causes increase of a consumption electric current and the behavior that are instability. Please fix an unused input terminal to the voltage that is near to V_{IO} or GND.

2) Notes on packaging

(1) Soldering heat resistance

If the temperature within the package exceeds +260°C, the characteristics of the crystal oscillator will be degraded, and it may be damaged. The reflow condition with our reflow profile is recommended. Therefore, always check the mounting temperature and time before mounting this device. Also, check again if the mounting conditions are later changed.

(2) Mounting equipment

While this module can be used with general-purpose mounting equipment, the internal crystal oscillator may be damaged in some circumstances, depending on the equipment and conditions. Therefore, be sure to check this. In addition, if the position for mounting later is changed, the same check should be performed again.

(3) Ultrasonic cleaning

Depending on the usage conditions, there is a possibility that the crystal oscillator will be damaged by resonance during ultrasonic cleaning. Since the conditions under which ultrasonic cleaning is carried out (the type of cleaner, power level, time, the distance of the cleaning vessel, etc.) vary widely, this device is not warranted against damage during ultrasonic cleaning.

(4) Mounting orientation

This device can be damaged if it is mounted in the wrong orientation. Always confirm the orientation of the device before mounting.

(5) Leakage between pins

It may occur if the mounted device is turned on while the device has condensation or dirt on it. Make sure the device is dry and clean before supplying power to it.

(6) Installation of charged battery

When a charged backup battery is installed by soldering, battery connection terminal of this device should connect to GND, beforehand.

13. Overview of Functions and Registers

Note: The initialization of the register is necessary about the unused function.

13.1. Overview of Functions

1) Clock functions

This function is used to set and read out second, minute, hour, day, month, year (to the last two digits), and date data.

Any (two-digit) year that is a multiple of 4 is treated as a leap year and calculated automatically as such until the year 2099.

At the start of a I²C communication, the time and clock counting stops (which causes loss of time), and clock starts automatically again at the end of the I²C communication.

2) Wakeup Timer Interrupt function

The wakeup timer interrupt function generates an interrupt event periodically at any wakeup set between 244.14μs and 65535 hours.

When an interrupt event is generated, the /IRQ pin goes to Low level and "1" is set to the TF bit to report that an event has occurred.

3) Long-Timer function

It is able to use wakeup timer interrupt function as Long-Timer or usage counter.

The external MCU accumulates the operating duration by the timer under main power and/or backup power. Based on the register configuration, it can automatically sum the total operating time or selectively sum only the main-power operation time or only the backup-power operation time. The external MCU/CPU has to accumulate every overflow from polling the TF bit or the interrupting signal from /IRQ for the calculation of the specific long-term usage time. The resolution of timer can be from 244.14μs to 1 hour.

4) Alarm interrupt function

The alarm interrupt function generates interrupt events for alarm settings such as date, day, hour, and minute settings. When an interrupt event occurs, the AF bit value is set to "1" and the /IRQ pin goes to low level to indicate that an event has occurred.

5) Time Update Interrupt Function

The time update interrupt function generates interrupt in one-second or one-minute intervals which are synchronized to the update of the second or minute time register of the RTC. When an interrupt event is generated, the /IRQ pin goes to low level and "1" is set to the UF bit to report that an event has occurred.

6) Frequency stop detection function

VLF indicates the retained status of clock operations or internal data. Its value changes from "0" to "1" when data loss might have occurred due to a low supply voltage.

7) Clock output function

A clock with the same frequency (32.768 kHz) as the built-in crystal resonator can be output from the FOUT pin. Output could also be 1 Hz, or 1024 Hz.

8) User RAM

RAM register is read/write accessible for any data.

9) Digital offset function

The clock precision can be increased by adding a time offset.

13.2. Register Table

13.2.1. Register Table

Address h	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
10	SEC	0	40	20	10	8	4	2	1
11	MIN	0	40	20	10	8	4	2	1
12	HOUR	0	0	20	10	8	4	2	1
13	WEEK	0	6	5	4	3	2	1	0
14	DAY	0	0	20	10	8	4	2	1
15	MONTH	0	0	0	10	8	4	2	1
16	YEAR	80	40	20	10	8	4	2	1
17	MIN Alarm	AE	40	20	10	8	4	2	1
18	HOUR Alarm	AE	•	20	10	8	4	2	1
19	WEEK Alarm	AE	6	5	4	3	2	1	0
	DAY Alarm		•	20	10	8	4	2	1
1A	Timer Counter 0	128	64	32	16	8	4	2	1
1B	Timer Counter 1	32768	16384	8192	4096	2048	1024	512	256
1C	Extension Register	FSEL 1	FSEL 0	USEL	TE	WADA	TSEL 2	TSEL 1	TSEL 0
1D	Flag Register	VBLF	0	UF	TF	AF	RSF	VLF	VBFF
1E	Control Register0	<u>TEST</u>	STOP	UIE	TIE	AIE	TSTP	TBKO N	TBKE
1F	Control Register1	SMP TSEL 1	SMP TSEL0	CHG EN	INIEN	0	RS VSEL	BF VSEL1	BF VSEL 0

Address h	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
20 23	RAM	User Register 32 bits (4-word x 8 bit)							

Address h	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
30	Digital offset	DTE	L7	L6	L5	L4	L3	L2	L1
31	Extension Register1	-	-	-	-	-	-	-	VBLF E

Table 13 Register Table

After the initial power-up (from 0V) or in case the VLF bit returns "1", make sure to initialize all registers, before using the RTC.

Be sure to avoid entering incorrect date and time data, as clock operations are not guaranteed when the data or time data is incorrect.

The TEST bit is used by the manufacturer for testing. Be sure to set "0" for this bit when writing.

* Be sure to write "0" by initializing before using the clock module. Afterward, be sure to set "0" when writing

"0" means that writing is invalid and the read value is always 0.

Any bit marked with "•" is a RAM bit that can be used to read or write any data.

User Register is a free register which can be used as user RAM.

The above table shows only the user registers. Due to functional reasons, RTC has different registers not mentioned above table which are programmed by the manufacturer. Please make sure to only access above mentioned user registers.

“-“ bit is TEST bit. During initialization, it must be set to ‘0’ and kept at ‘0’

13.2.2. Register initial value and Read/Write operation Table

After power-on-reset, registers bits of RTC are configured automatically as below. The value will be the same even after Software Reset is executed.

[X: Undefined in 0 or 1. Usually, it keeps data of before Power-On-Reset.]
 [0: Reset state]
 [1: Set state]

Address h	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
10	SEC	0	X	X	X	X	X	X	X
11	MIN	0	X	X	X	X	X	X	X
12	HOURL	0	0	X	X	X	X	X	X
13	WEEK	0	X	X	X	X	X	X	X
14	DAY	0	0	X	X	X	X	X	X
15	MONTH	0	0	0	X	X	X	X	X
16	YEAR	X	X	X	X	X	X	X	X
17	MIN Alarm	X	X	X	X	X	X	X	X
18	HOURL Alarm	X	X	X	X	X	X	X	X
19	WEEK Alarm	X	X	X	X	X	X	X	X
	DAY Alarm		X	X	X	X	X	X	X
1A	Timer Counter 0	X	X	X	X	X	X	X	X
1B	Timer Counter 1	X	X	X	X	X	X	X	X
1C	Extension Register	0	0	0	0	0	1	0	0
1D	Flag Register	0	0	0	0	0	1	1	0
1E	Control Register0	0	0	0	0	0	0	0	0
1F	Control Register1	0	0	0	0	0	0	0	0

Address h	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
20-23	RAM	X	X	X	X	X	X	X	X

Address h	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
30	Digital offset	0	0	0	0	0	0	0	0
31	Extension Register1	0	0	0	0	0	0	0	0

Table 14 Register initial value, Read/Write

13.3. Description of registers

13.3.1. Clock and calendar registers (0h ~ 16h)

This is counter registers from a second to a year.
See [\[14.1 Clock calendar explanation\]](#) for details.

13.3.2. RAM registers (20h ~ 23h)

This RAM register is read/write accessible for any data in the range from 00h to FFh.

13.3.3. Alarm registers (17h ~ 19h)

The alarm interrupt function is used, along with the AE, AF, and WADA bits, to set alarms for specified date, day, hour, and minute values.
See [\[14.3. Alarm Interrupt Function\]](#) for the details.

13.3.4. Timer setting and Timer counter register for wakeup timer (1Ah ~ 1Eh)

This register is used to set the default (preset) value for the counter.
To use the wakeup timer interrupt function, TE, TF, TIE, TSEL2, TSEL1, TSEL0, TBKON, TBKE bits are set and used. When the wakeup timer interrupt function is not being used, the wakeup timer control register can be used as a RAM register. In such cases, stop the wakeup timer function by writing "0" to the TE and TIE bits.
See [\[14.2. Wakeup Timer Interrupt Function\]](#) for the details.

13.3.5. Function-related register 1 (1Ch ~ 1Eh)

1) FSEL1, FSEL0 bit

A combination of the FSEL1 and FSEL0 bits are used to select the frequency to be output. By combining the FSEL bits with the CE/FOE pin, you can select the clock-output frequency or disable the clock output.
See [\[14.6. FOUT Function\]](#) for the details.

2) USEL, UF, UIE bit

This bit is used to specify either "second update" or "minute update" as the update generation timing of the time update interrupt function.
See [\[14.4. Update interrupt function\]](#) for the details.

3) TE, TF, TIE, TSEL2, TSEL1, TSEL0, TSTP, TBKON, TBKE bit

These bits are used to control operation of the wakeup timer interrupt function.

4) WADA, AF, AIE bit

These bits are used to control operation of the alarm interrupt function.

5) TEST bit

These bits are the manufacturer's test bit. Always leave this bit value as "0"..

6) VLF bit

This flag bit indicates the retained status of clock operations or internal data. Its value changes from "0" to "1" when data loss occurs, such as due to a supply voltage drop.
See [\[14.5. Frequency stop detection function\]](#) for the details.

7) STOP bit

This bit is to stop a timekeeping operation. In the case of "STOP bit = 1":

- 1) All the update of timekeeping and the calendar operation stops.

With it, an update interrupt event does not occur at an alarm or the time update interrupts.

2) Part of the wakeup-timer interrupt function is halted.

If the timer's source clock is set to 64 Hz, 1 Hz, 1 minute, or 1 hour, the timer will stop counting.

3) The effect of STOP bit to FOUT functions.

When STOP = "1", 32.768 kHz and 1024 Hz output is possible. But 1 Hz output is disabled.

4) The switchover function does not operate because VDD-voltage-drop detection is disabled, even if the main power supply falls.

8) RSF bit

This flag bit holds the result of detecting the reset voltage ($-V_{DET1}$) at V_{DD} .

13.3.6. Function-related register 2 (1Fh)

1) SMPTSEL1, SMPTSEL0 bit

Operation time setting of a voltage detector circuit for each power supply pin.

See [\[15.1. Description of Battery Backup switchover function\]](#) for the details.

2) CHGEN bit

Setting of backup battery charge control (ON/OFF).

3) INIEN bit

Setting of a power switchover function (ON/OFF).

4) RSVSEL bit

Setting of voltage detection level of a V_{DD} pin.

5) BFMSEL1, BFMSEL0 bit

Setting of the full charge detection voltage of a backup battery.

13.3.7. Digital offset register (30h)

1) DTE bit

Setting of a Digital offset function (ON/OFF).

See [\[17. Digital offset function\]](#) for the details.

2) L7 ~ L1 bit

Setting of a Digital offset value.

14. Functions

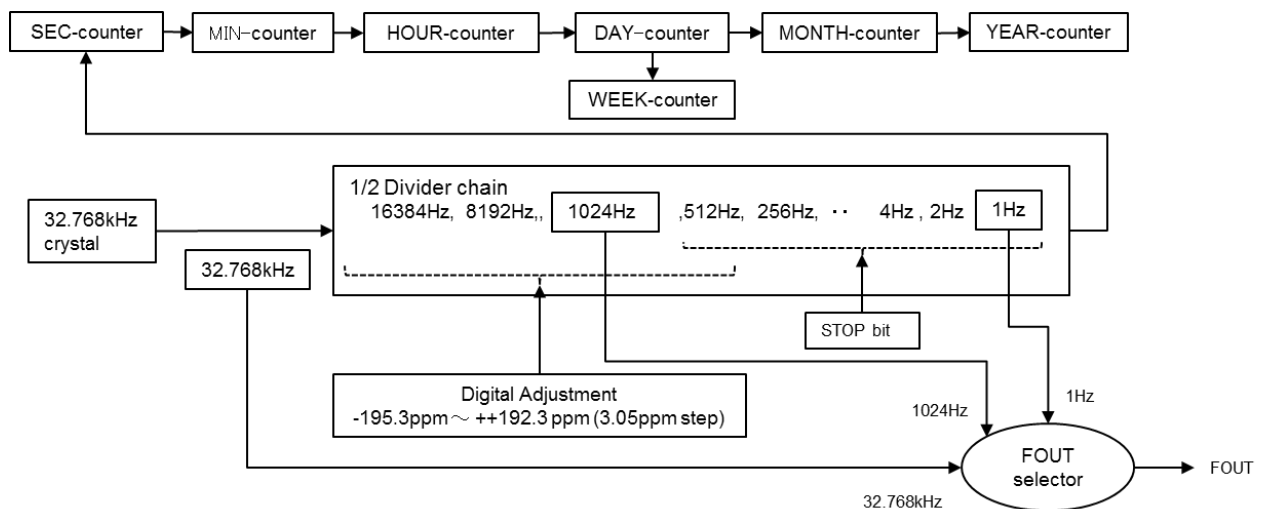


Figure 19 Basic (32.768 k Hz oscillation, counter, FOUT) Function

14.1. Clock calendar explanation

The device freezes (holds) its timekeeping registers at the start of a communication session. This creates a fixed snapshot of the Clock & Calendar values. The registers remain held during the entire transaction and are refreshed only when the communication ends. Because the snapshot does not update until the transaction finishes, it is recommended to access the Clock & Calendar registers in one continuous sequence using the device's auto-increment mechanism.

Address h	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
10	SEC	0	1	0	0	0	1	0	1
11	MIN	0	0	1	1	1	0	0	1
12	HOUR	0	0	0	1	0	1	1	1
13	WEEK	0	0	0	0	0	0	0	1
14	DAY	0	0	1	0	1	0	0	1
15	MONTH	0	0	0	0	0	0	1	0
16	YEAR	1	0	0	0	1	0	0	0

*Note with caution that writing non-existent time data may interfere with normal operation of the clock counter.

Table 15 Time, calendar setting example (Sun, 29-Feb-88 17:39:45 (leap year))

14.1.1. Clock counter

1) [SEC][MIN]register

These registers are 60-base BCD counters. These registers are incremented at the timing when carry is generated from a lower register. At the timing when the lower register changes from 59 to 00, carry is generated to the higher register and thus incremented.

When writing is performed to [SEC] register, Internal-count-down-chain less than one second (512 Hz~1Hz) is cleared to 0.

2) [HOUR] register

This register is a 24-base BCD counter (24-hour format). These registers are incremented at the timing when a carry is generated from a lower register ([MIN]register).

14.1.2. Week counter

The day (of the week) is indicated by 7 bits, bit 0 to bit 6.

The day data values are counted as: Day 01h→Day 02h→Day 04h→Day 08h→Day 10h→Day 20h→Day 40h→Day 01h→Day 02h, etc.

It is incremented when carry is generated from the HOUR register. This register does not generate carry to a higher register. Since this register is not connected with the YEAR, MONTH and DAY registers, it needs to be set again with the matching day of the week if any of the YEAR, MONTH or DAY registers have been changed.

Day	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0	Data h
Sunday	0	0	0	0	0	0	0	1	01 h
Monday	0	0	0	0	0	0	1	0	02 h
Tuesday	0	0	0	0	0	1	0	0	04 h
Wednesday	0	0	0	0	1	0	0	0	08 h
Thursday	0	0	0	1	0	0	0	0	10 h
Friday	0	0	1	0	0	0	0	0	20 h
Saturday	0	1	0	0	0	0	0	0	40 h

*Do not set "1" to more than one day at the same time.

Table 16 Setting example of the week register value.

14.1.3. Calendar counter

1) [DAY],[MONTH] register

The DAY register is a variable (between 28-base and 31-base) BCD counter that is influenced by the month and the leap year. The MONTH register is a 12-base BCD counter triggered by carryover of the day register.

		Ja n.	Fe b.	Ma r	Ap r.	Ma y	Ju ne	Jul y	Au g.	Se p.	Oc t.	No v.	De c.
Days	Comm on year		28										
	Leap year	31	29	31	30	31	30	31	31	30	31	30	31

2) [YEAR]register

This register is a BCD counter for years 00 to 99.

The leap year is automatically determined and influences the DAY register.

This RTC processes following years as leap years: 00, 04, 08, 12, ..., 96.

User software correction is needed in the years 2100, 2200, 2300, etc. as they are common years.

Under the Gregorian calendar rules, a year is a leap year if:

1. It is divisible by 4,
2. Except if it is divisible by 100, unless it is also divisible by 400.

< Definition of leap years>

- Leap year: year divisible by 4, year divisible by 400
Ex. 2000, 2004, 2008, 2012, ..., 2096, 2400, 2800,
- Common year: year indivisible by 4, year divisible by 100
Ex. 2001, 2002, 2003, 2005, ..., 2099, 2100, 2200, 2300, 2500,

14.2. Wakeup Timer Interrupt Function

The wakeup timer interrupt function generates an interrupt event periodically at any wakeup set between 244.14 μ s and 65535 hours. This function can stop at one time and is available as an accumulative timer.

After the interrupt occurs, the /IRQ outputs is released in tRTN2 automatically

14.2.1. Related registers for function of wakeup timer interrupt function

Address h	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1A	Timer Counter 0	128	64	32	16	8	4	2	1
1B	Timer Counter 1	32768	16384	8192	4096	2048	1024	512	256
1C	Extension Register	FSEL 1	FSEL 0	USEL	TE	WAD A	TSEL 2	TSEL1	TSEL 0
1D	Flag Register	VBLF	0	UF	TF	AF	RSF	VLF	VBFF
1E	Control Register0	<u>TEST</u>	STOP	UIE	TIE	AIE	TSTP	TBKO N	TBK E

Before entering operation settings, we recommend first resetting the TE bit to "0". When the wakeup timer function is not being used, the wakeup Timer Counter0,1 register can be used as a RAM register. In such cases, stop the wakeup timer function by writing "0" to the TE and TIE bits.

1) Down counter for wakeup timer (Timer Counter 1, 0)

This register is used to set the default (preset) value for the counter. Any count value from 1(0001h) to 65535(FFFFh) can be set.

Be sure to write "0" to the TE bit before writing the preset value.

When TE=0, read out data of timer counter is default (Preset) value.

And when TE=1, read out data of timer counter is counting down value.

But when access to timer counter data, counting value is not held.

It is recommended to read the full 16-bit value (Timer Counter 0 and 1) twice and use it only if both reads match.

2) TSEL2, TSEL1, TSEL0 bit

The combination of these three bits is used to set the countdown period (source clock) for this function.

TSEL2 (bit 2)	TSEL1 (bit 1)	TSEL0 (bit 0)	Source clock		Auto release time tRTN2 (Min.)
0	0	0	4096Hz	/Once per 244.14 μ s	122 μ s
0	0	1	64Hz	/Once per 15.625 ms	7.57ms
0	1	0	1Hz	/Once per second	7.57ms
0	1	1	1/60Hz	/Once per minute	7.57ms
1	0	0	1/3600 Hz	/Once per hour	7.57ms

Table 17 Countdown period (source clock) selection

The /IRQ pin's auto reset time (t_{RTN}) varies as shown above according to the source clock setting.

The first countdown is shorter than a source clock. It occurs at the 1st rising edge of the internal clock after enabling the timer.

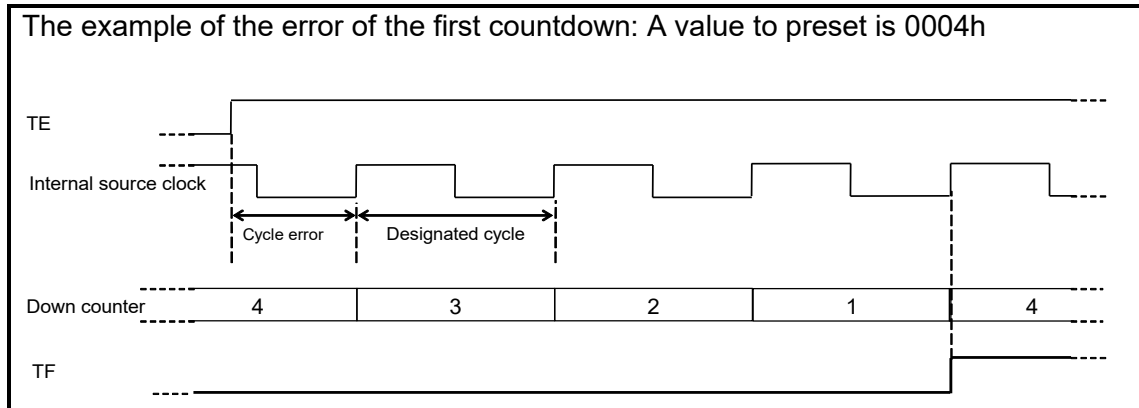


Figure 20 Wakeup timer initial sequence

When selected 4,096 Hz / 64 Hz / 1Hz as a source clock, one period of error occurs at the maximum.

When selected 1/60 Hz / 1/3600 Hz as a source clock, 1 Hz of error occurs at the maximum given that 1Hz is the minimum resolution for these two source frequencies.

Inside counter block diagram

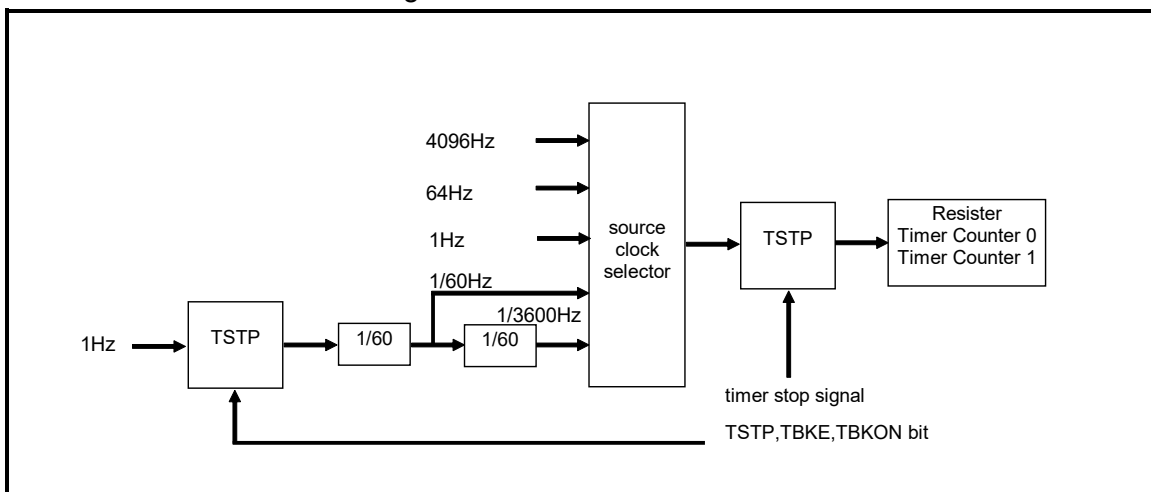


Figure 21 Wakeup timer block diagram

Note: The resolution of the count value depends on the source clock

3) TE bit (Timer Enable)

TE bit is used for starting or stopping the Timer.

When TE bit is "0", the preset value of the timer can be checked by reading this register.

TE	Data	Description
Write	0	The wakeup timer interrupt function is stopped. The wakeup timer interrupt output is released to Hi-Z immediately. Preset values are loaded on timer counter 0 and 1. New preset values can be set for timer counter 0 and 1.
	1	The wakeup timer interrupt function starts operating. When TE is set from 0 to 1, the timer counter starts counting down from the preset value.

Table 18 Wakeup timer control

4) TF bit (Timer Flag)

This is a flag bit that retains the result when a wakeup timer interrupt event is occurred.

TF	Data	Description
Write	0	The /IRQ low output is released immediately.
	1	Invalid (writing a 1 will be ignored)
Read	0	Wakeup timer interrupt did not occur.
	1	Wakeup timer interrupt did occur. Result is retained until this bit is cleared to zero.

Table 19 Wakeup timer interrupt detection flag

5) TIE bit (Timer Interrupt Enable)

This bit is used to control output of interrupt signals from the /IRQ pin when a wakeup timer interrupt event has occurred.

TIE	Data	Description
Write	0	1) Even if wakeup timer interrupt event occurs, an interrupt signal is not generated. 2) When a /IRQ was output Wakeup timer interruption already, the wakeup timer interrupt signal is released to Hi-Z from low.
	1	When a wakeup timer interrupt event occurs, an interrupt signal is generated (/IRQ status changes to low from Hi-Z).

Table 20 Wakeup timer interrupt control

6) TBKON, TBKE bit

This function selects the operation time with the main power supply or the operation time with the backup power supply. The count value is added.

operation	TBKE	TBKON	Description
Write	0	X	This setting counts normal mode and backup mode.
	1	0	This setting counts it at time of normal mode (VDD operation)
		1	This setting counts it at time of backup mode (VBAT operation)

Table 21 Wakeup timer normal mode/backup mode control

7) TSTP bit (Timer Stop)

This bit is used to enable/disable the restarting to countdown the wakeup timer.

TE	STOP	TBKE	TSTP	Description
1	0	0	0	Countdown is restarted. The restart value of the countdown is a stopping value
			1	Count stops.
		1	X	Setting TSTP value becomes invalid, and the count does not stop even if TSTP sets to 1.
	1	X	X	When source clock is 64 Hz, 1 Hz, 1/60 Hz, 1/3600 Hz, the countdown is stopped.
0	X	X	X	The preset value is loaded to timer counter 1, 2. Timer countdown is stopped.

Table 22 Wakeup timer stop control

14.2.2. Wakeup timer start timing

When the TE value is changed from "0" to "1", counting down of the wakeup timer value starts at the rising edge of the SCL following the ACK output from SDA.

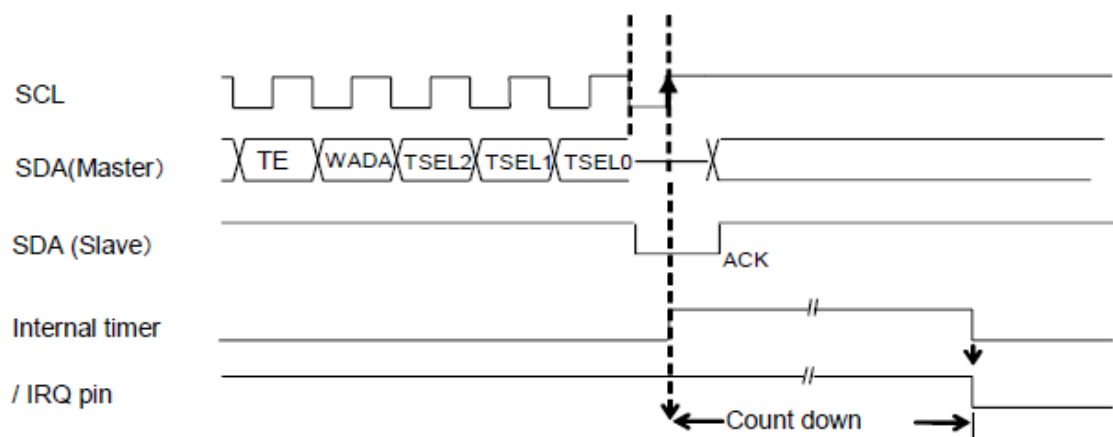


Figure 22 Wakeup timer start sequence

14.2.3. Wakeup timer interrupt interval

The combination of the source clock settings and wakeup timer countdown setting determines the interrupt interval, as shown in the following table.

Timer Counter setting 1~65535	Source clock				
	4096 Hz TSEL2=0 TSEL1,0=0,0	64 Hz TSEL2=0 TSEL1,0=0,1	1Hz TSEL2=0 TSEL1,0=1,0	1/60 Hz TSEL2=0 TSEL1,0=1,1	1/3600 Hz TSEL2=1 TSEL1,0=0,0
0	—	—	—	—	—
1	244.14 μs	15.625 ms	1 s	1 min	1 h
•	•	•	•	•	•
410	100.10 ms	6.406 s	410 s	410 min	410 h
•	•	•	•	•	•
•	•	•	•	•	•
3840	0.9375 s	60.000 s	3840 s	3840 min	3840 h
•	•	•	•	•	•
•	•	•	•	•	•
4096	1.0000 s	64.000 s	4096 s	4096 min	4096 h
•	•	•	•	•	•
•	•	•	•	•	•
65535	15.999 8 s	1023.9 84 s	65535 s	65535 min	65535 h

Table 23 Wakeup timer interrupt cycles

14.2.4. Diagram of wakeup timer interrupt function

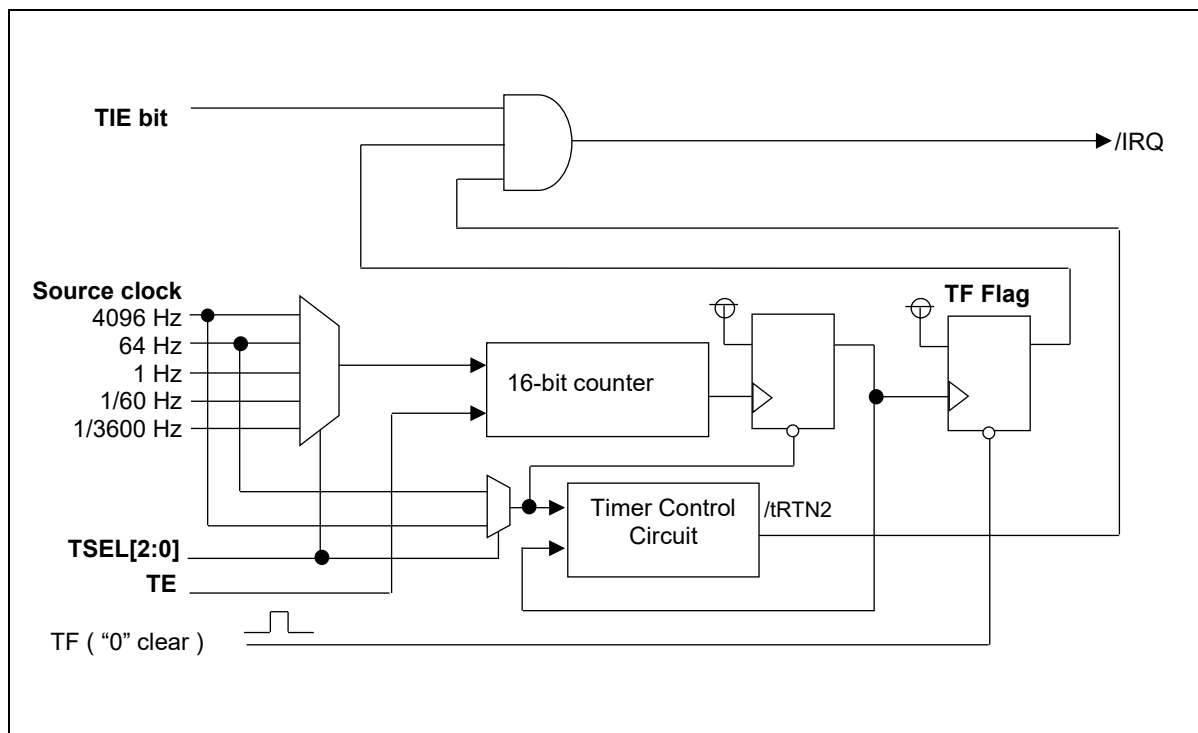


Figure 23 Wakeup timer inner block diagram

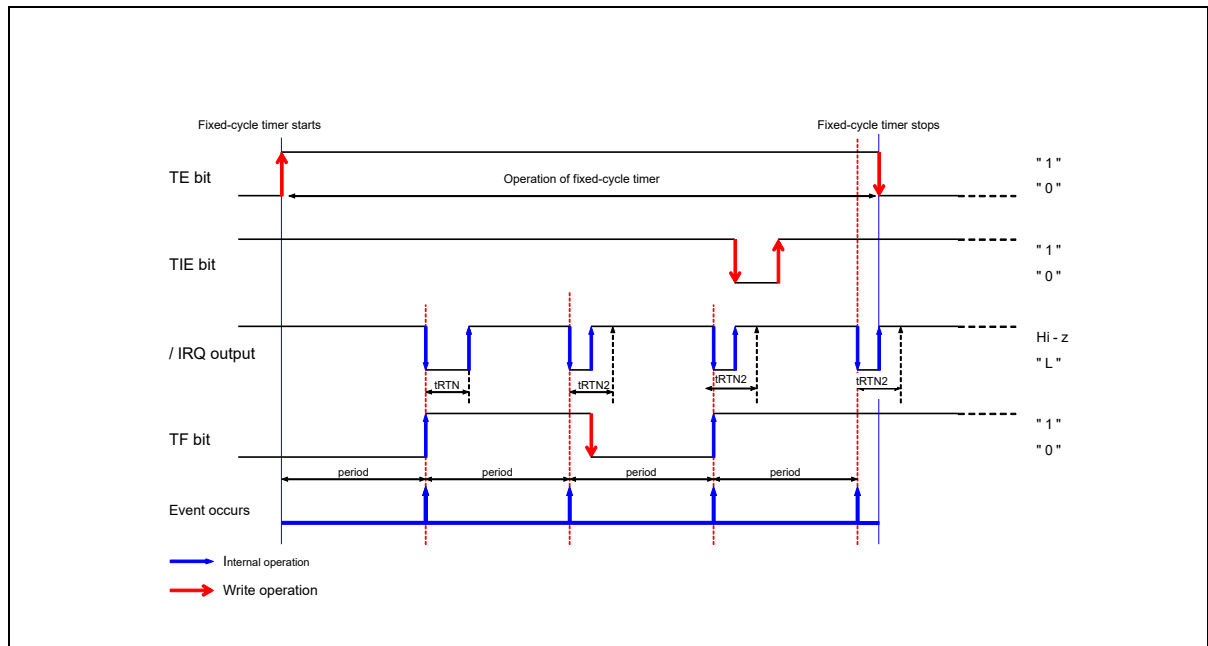


Figure 24 Wakeup timer timing chart

14.3. Alarm Interrupt Function

The alarm interrupt function generates interrupt events for alarm settings combined with date, day, hour, and minute settings.

When an interrupt event occurs, the AF bit value is set to "1" and the /IRQ pin goes to low level to indicate that an event has occurred. AF bit and /IRQ output show a maximum delay of 1.46ms from the alarm event.

* /IRQ pin remains at the "L" level when an alarm interrupt occurs, and it will not clear automatically. It stays Low until the interrupt is intentionally cancelled by software.

14.3.1. Related registers for Alarm interrupt functions.

Address h	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
17	MIN Alarm	AE	40	20	10	8	4	2	1
18	HOUR Alarm	AE	•	20	10	8	4	2	1
19	WEEK Alarm	AE	6	5	4	3	2	1	0
	DAY Alarm		•	20	10	8	4	2	1
1C	Extension Register	FSEL 1	FSEL 0	USEL	TE	WAD A	TSEL 2	TSEL 1	TSEL 0
1D	Flag Register	VBLF	0	UF	TF	AF	RSF	VLF	VBFF
1E	Control Register0	TEST	STOP	UIE	TIE	AIE	TSTP	TBKO N	TBKE

* Before entering settings for operations, we recommend writing a "0" to the AIE bit to prevent hardware interrupts from occurring inadvertently while entering settings.

* When the STOP bit value is "1" alarm interrupt events do not occur.

* When the alarm interrupt function is not being used, the Alarm registers (Reg – 17h to 19h) can be used as a RAM register. In such cases, be sure to write "0" to the AIE bit.

* When the AIE bit value is "1" and the Alarm registers (Reg – 17h to 19h) is being used as a RAM register, /IRQ may be changed to low level unintentionally.

1) AE bit

The minute, hour, day, and date at which an alarm interrupt event occurs are configured through the corresponding AE bits together with the WADA bit.

In the WEEK alarm /Day alarm register (Reg – 19h), the setting selected via the WADA bit determines whether WEEK alarm data or DAY alarm data will be set. If WEEK has been selected via the WADA bit, multiple days can be set (such as Monday, Wednesday, Friday, Saturday).

When the settings made in the alarm registers and the WADA bit match the current time, the AF bit value is changed to "1". At that time, if the AIE bit value has already been set to "1", the /IRQ pin goes low.

Note: AE-bit is low active, so in order to enable 1 interrupt every hour once the actual minutes match the alarm setting, it is necessary to set the AE of register 17h to 0 and the AE of 18h and 19h to 1.

In order to generate an alarm interrupt only once a week, all 3 AE-bits have to be set "0"

*1) The alarm function is not a HW feature but software function inside the RTC.

*2) In case "AE" bit of register 19h is set to "1", the day will be ignored, and an interrupt occurs once the actual time matches the minutes and/or hour setting of the alarm register.

(Example) Write 80h (AE = "1") to the WEEK Alarm /DAY Alarm register (Reg - 19h): Only the hour and minute settings are used as alarm comparison targets. The week and date settings are not used as alarm comparison targets. As a result, alarm occurs if only the hour and minute values match the alarm data.

*3) If all three AE bit values are "1" the week/date and time settings are ignored, and an alarm interrupt event will occur once per minute.

2) WADA bit (Week Alarm / Day Alarm Select)

The alarm interrupt function uses either "Day" or "Week" as its target. The WADA bit is used to specify either WEEK or DAY as the target for alarm interrupt events.

WADA	Data	Description
Write	0	Sets WEEK as target of alarm function
	1	Sets DAY as target of alarm function

Table 24 WEEK/DAY control

3) AF bit (Alarm Flag)

When this flag bit value is already set to "0", occurrence of an alarm interrupt event changes it to "1". When this flag bit value is "1", its value is retained until a "0" is written to it.

AF	Data	Description
Write	0	Clearing this bit to zero enables /IRQ low output to be canceled (/IRQ remains Hi-z) when an alarm interrupt event has occurred.
	1	Invalid (writing a 1 will be ignored)!
Read	0	–
	1	Alarm interrupt events are detected. (Result is retained until this bit is cleared to zero.)

Table 25 Alarm Flag

4) AIE bit (Alarm Interrupt Enable)

This bit is used to control output of interrupt signals from the /IRQ pin when an Alarm interrupt event has occurred.

AIE	Data	Description
Write	0	1) When an alarm interrupt event occurs, an interrupt signal is not generated or is canceled (/IRQ status remains Hi-z). 2) When an alarm interrupt event occurs, the interrupt signal is canceled (/IRQ status changes from low to Hi-z).
	1	When an alarm interrupt event occurs, an interrupt signal is generated (/IRQ status changes from Hi-z to low).

Table 26 Alarm Interrupt control

The AIE bit is only output control of the /IRQ terminal. It is necessary to clear an AF flag to cancel alarm.

14.3.2. Examples of alarm settings

- 1) Example of alarm settings when "Week" has been specified (and WADA bit="0")

Week is specified WADA bit = "0"	Week Alarm								HOUR Alarm	MIN Alarm
	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0		
	AE	S	F	T	W	T	M	S		
Monday through Friday, at 7:00 AM * Minute value is ignored	0	0	1	1	1	1	1	0	07 h	AE bit = 1
Every Saturday and Sunday, for 30 minutes each hour * Hour value is ignored	0	1	0	0	0	0	0	1	AE bit = 1	30 h
Every day, at 6:59 PM	0	1	1	1	1	1	1	1	18 h	59 h
	1	X	X	X	X	X	X	X		

X: Don't care

Table 27 WEEK alarm example

- 2) Example of alarm settings when "Day" has been specified (and WADA bit="1")

Day is specified WADA bit = "1"	Day Alarm								HOUR Alarm	IN Alarm
	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0		
	AE	•	20	10	08	04	02	01		
First of each month, at 7:00 AM * Minute value is ignored	0	0	0	0	0	0	0	1	07 h	AE bit = 1
15 th of each month, for 30 minutes each hour * Hour value is ignored	0	0	0	1	0	1	0	1	AE bit = 1	30 h
Every day, at 6:59 PM	1	X	X	X	X	X	X	X	18 h	59 h

X: Don't care

Table 28 DAY alarm example

14.3.3. Diagram of alarm interrupt function

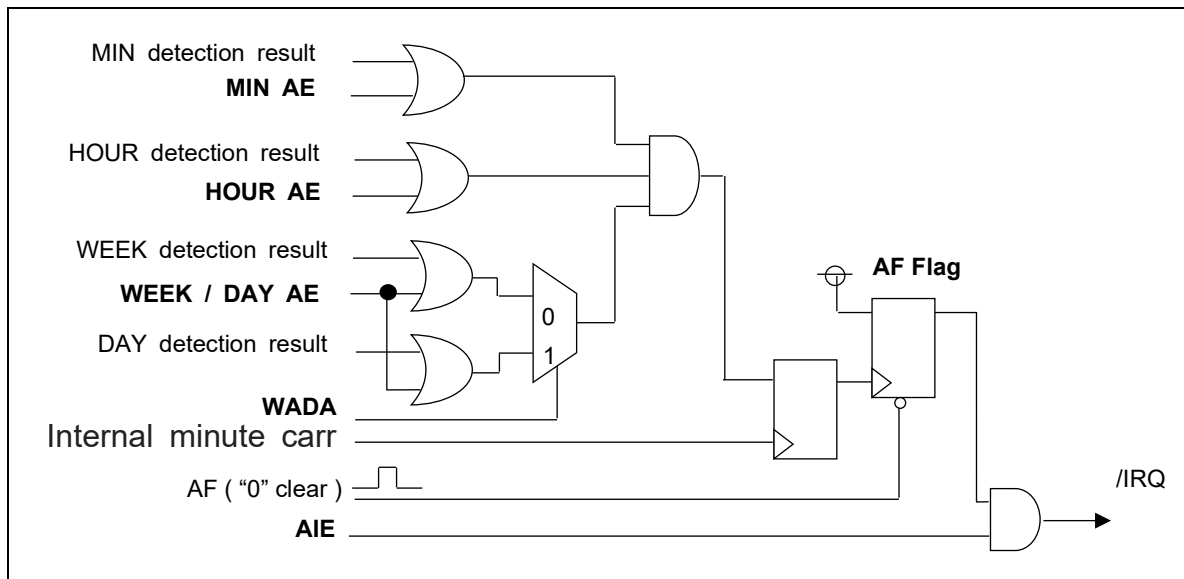


Figure 25 Alarm interrupt inner block diagram

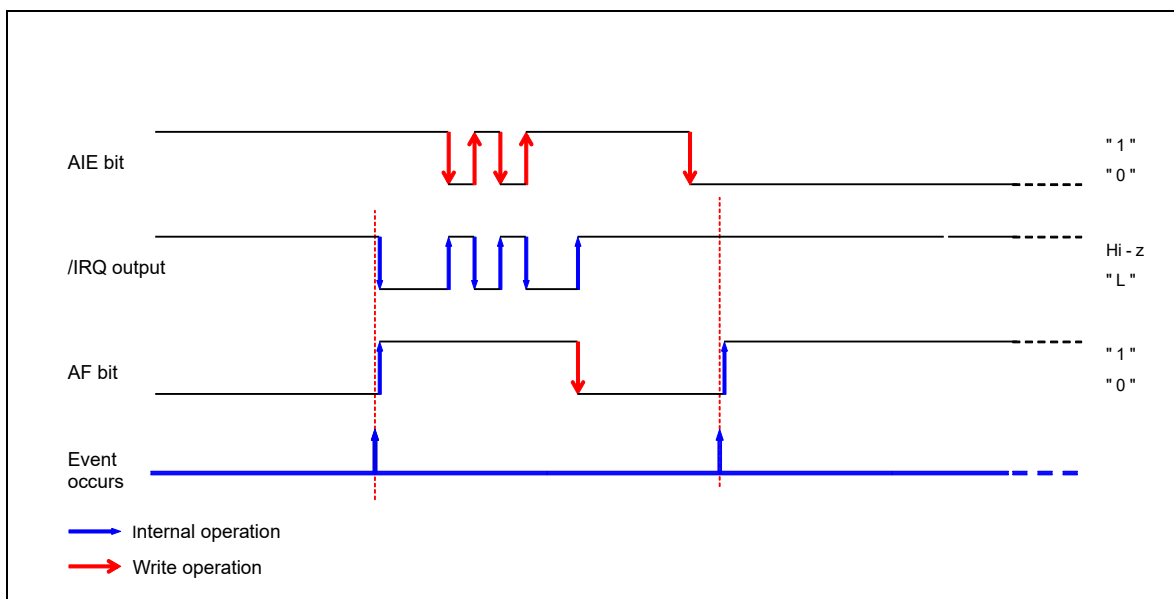


Figure 26 Alarm Interrupt time chart

14.4. Time Update Interrupt Function

The time-update interrupt generates an interrupt every second or minute, synchronized with the RTC's second or minute register update. The /IRQ status is automatically cleared (/IRQ status changes from low level to Hi-z earliest 7.57ms (maximum 15.63ms) after the interrupt occurs). This time width is auto release time (tRTN1).

14.4.1. Related registers for time update interrupt functions.

Address h	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1C	Extension Register	FSEL 1	FSEL 0	USEL	TE	WAD A	TSEL 2	TSEL 1	TSEL 0
1D	Flag Register	VBLF	0	UF	TF	AF	RSF	VLF	VBFF
1E	Control Register0	TEST	STOP	UIE	TIE	AIE	TSTP	TBKON	TBKE

* Before entering settings for operations, we recommend writing a "0" to the UIE bit to prevent hardware interrupts from occurring inadvertently while entering settings.

* When the STOP bit value is "1" time update interrupt events do not occur.

* Although the time update interrupt function cannot be fully stopped, if "0" is written to the UIE bit, the time update interrupt function can be prevented from changing the /IRQ pin status to low.

1) USEL bit (Update Interrupt Select)

This bit is used to select "second" update or "minute" update as the timing for generation of time update interrupt events.

UF bit(Update Flag) This flag bit value changes from "0" to "1" when a time update interrupt event occurs.

Table 29 Second/Minute selection

USEL	Data	Description
Write	0	Selects "second update" (once per second) as the timing for generation of interrupt events
	1	Selects "minute update" (once per minute) as the timing for generation of interrupt events

UF	Data	Description
Write	0	Clearing this bit to zero enables /IRQ low output of time update to be canceled immediately when a time update interrupt event has occurred.
	1	Invalid (writing a 1 will be ignored)
Read	0	—
	1	Time update interrupt events are detected. (The result is retained until this bit is cleared to zero.)

Table 30 Time update Flag

2) UIE bit (Update Interrupt Enable)

This bit selects whether to generate an interrupt signal or to not generate it.

UIE	Data	Description
Write / Read	0	1) Does not generate an interrupt signal when a time update interrupt event occurs. 2) Cancels interrupt signal triggered by time update interrupt event. Even when the UIE bit value is "0" another interrupt event may change the /IRQ status to low (or may hold /IRQ = "L").
	1	When a time update interrupt event occurs, an interrupt signal is generated (/IRQ status changes from Hi-Z to low). * When a time update interrupt event occurs, low-level output from the /IRQ pin occurs only when the UIE bit value is "1". Earliest 7.57ms after the interrupt occurs, the /IRQ status is automatically cleared (/IRQ status changes from low to Hi-Z).

Table 31 Time update interrupt control

14.4.2. Time update interrupt function diagram

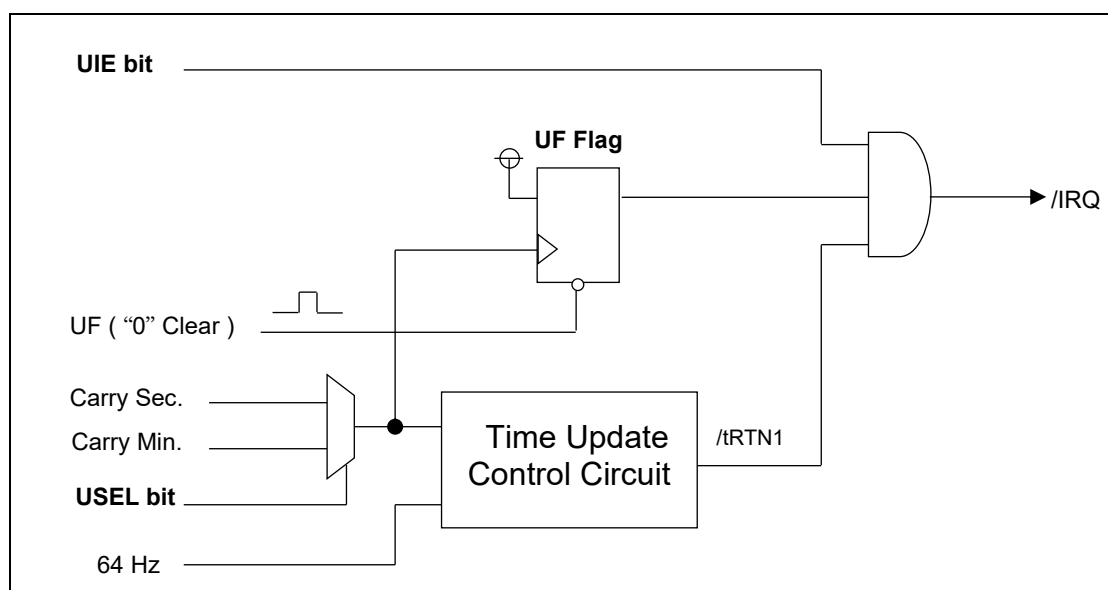


Figure 27 Time update inner block diagram

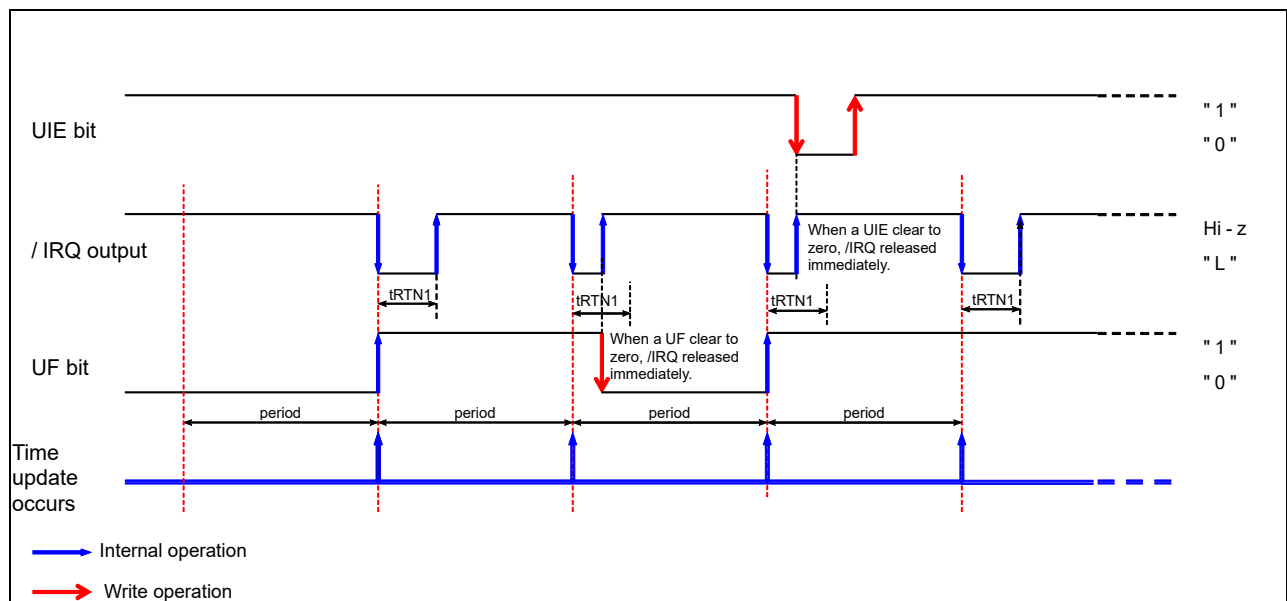


Figure 28 Time update time chart

14.5. Oscillation stop detection function

This flag bit (VLF) indicates the retained status of clock oscillation stop. Its value changes from "0" to "1" when data loss might have occurred due to clock oscillation stop, power on resetting. Once this flag bit's value is "1", its value is retained until a "0" is written to it. During the initial power-on (from 0V) and/or if the value of the VLF bit is "1", be sure to initialize all registers before using them.

14.5.1. Related registers for Oscillation stop and Voltage low detect function.

Address h	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1D	Flag Register	VBLF	0	UF	TF	AF	RSF	VLF	VBFF

VLF bit

VLF	Data	Description
Write	0	The VLF is cleared to 0 and waiting for next low voltage detection.
	1	Invalid (writing 1 will be ignored)
Read	0	Oscillation status is normal, RTC register data are valid.
	1	Oscillation stop is detected, RTC register data are invalid. Should be initialized of all register data. VLF is maintained till it is cleared by zero.

Table 32 Oscillation stop detection flag

14.6. FOUT function

The clock signal can be output via the FOUT pin. Output is stopped upon detection of the voltage drop below VDET1. In this case pin output becomes Hi-z.

14.6.1. FOUT control register.

Address h	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1C	Extension Register	FSEL 1	FSEL 0	USEL	TE	WAD A	TSEL 2	TSEL 1	TSEL 0

14.6.2. FOUT function Table.

FSEL1, FSEL0 bit

FSEL1	FSEL0	output
0	0	32.768kHz Output
0	1	1024Hz Output
1	0	1Hz Output
1	1	OFF

Table 33 FOUT Frequency selection

At the time of the initial power-on, "0" is set to FSEL1, FSEL0 by Power-On-Reset..

Note: The effect of STOP bit to FOUT functions.
 When STOP = "1", 32.768 kHz and 1024 Hz output is possible.
 But 1 Hz output is disabled.

15. Battery backup switchover function

15.1. Description of Battery backup switchover function

This function consists of a supply voltage detector "VDET" which detects if the supply voltage of the main power source connected to "VDD" drops below a threshold (V_{DET2}), and three MOS switches (SW1, SW2A and SW2B) located between the main power-source pin "VDD" and the backup power supply pin "VBAT". (Figure 29 Battery backup switchover block diagram)

The MOS-switches SW1, SW2A and SW2B are activated according to the result of the supply-voltage detection of VDET2 and the RTC changes the operating modes between normal mode (RTC power supply = V_{DD}) or backup mode (RTC power supply = V_{BAT}).

The RTCs backup function is built in a way to prevent reverse current flow from V_{BAT} to V_{DD} . While in backup-mode, the I2C-bus and FOUT function are switched off and related terminals switched to Hi-Z.

The figure below shows the switch status after power-on reset in the image of the power switching circuit.

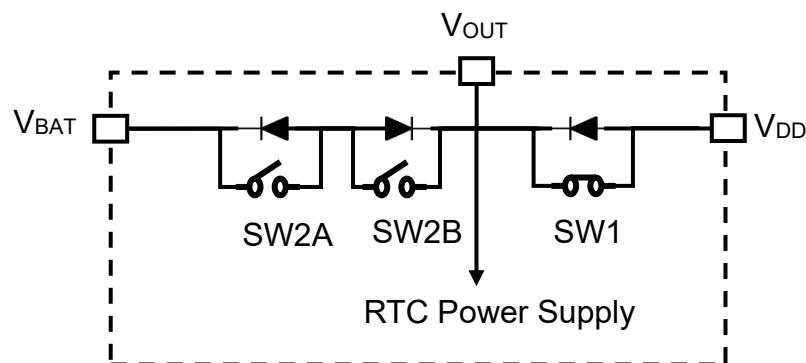


Figure 29 Battery backup switchover block diagram

15.1.1 Default power switch state

After a power-on reset, the power switch states are as follows:

SW1: Enabled (ON)

SW2A: Disabled (OFF)

SW2B: Disabled (OFF)

VDET2 Voltage Monitoring: Disabled (OFF).

In this state, no power switching occurs, and the system is powered exclusively by the VDD supply.

15.2. Reference characteristics of switching elements.

Item	Value	Condition
Limit of current.	40 mA Max.	SW1 = SW2A = SW2B = ON, +25 °C
Diode Vf Vf / Sink Current	0.40 V / 1 μ A Typ. 0.70 V / 1 mA Typ. 0.9 V / 10 mA Typ.	+25 °C
Diode IR	5 nA Max.	VR = 5.5 V, -40 °C ~ +85 °C

Table 34 Reference characteristics of switching elements.

When using a secondary battery, EDLC, please keep charge current 40 mA or less.

15.3. Reference characteristics of the charge current

Graph shows an electric current characteristic (Resistance characteristics of all ON of SW1, SW2B, SW2A) that can charge a second battery.

It is reference value in 25°C.

When V_{DD} voltage is high, the charge current increases.

And when little voltage differences of V_{DD} and V_{BAT} , charge current decreases.

A vertical axis shows charge current I_{chg} and a horizontal axis shows voltage difference V_{def} between V_{DD} and V_{BAT} .

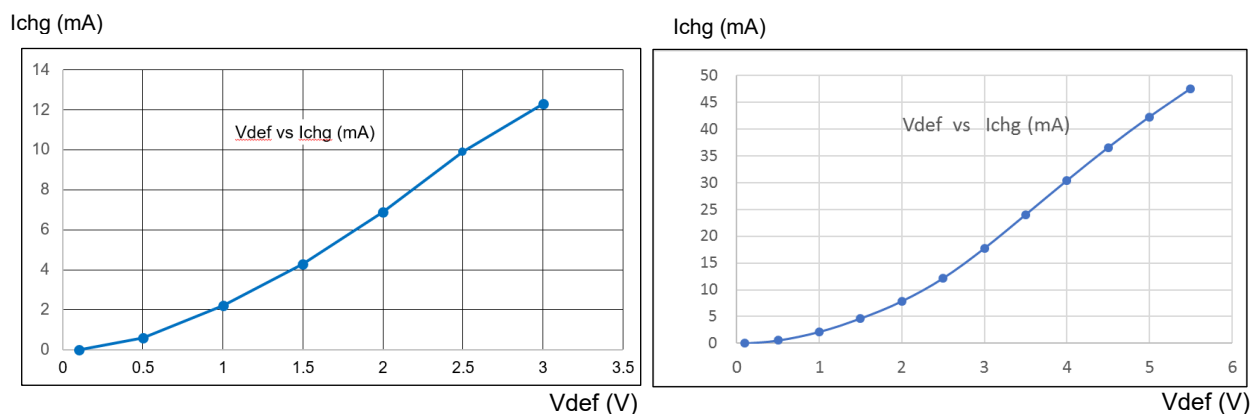


Figure 30 V_{BAT} charge current characteristics $V_{DD} = 3.0$ V, 5.5 V

15.4. Re-Chargeable battery Voltage Current features

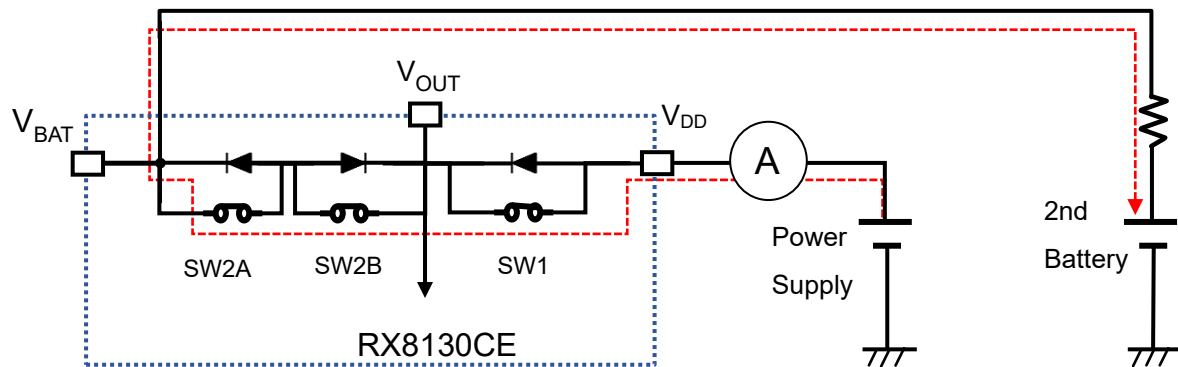


Figure 31 Re-chargeable battery connection

15.5. Related register of Battery backup switchover function

Address h	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1D	Flag Register	VBLF	0	UF	TF	AF	RSF	VLF	VBFF
1F	Control Register1	SMP TSEL 1	SMP TSEL0	CHG EN	INIEN	0	RS VSEL	BF VSEL1	BF VSEL 0

1) CHGEN bit

This bit has to be set to allow charging of a Re-chargeable battery connected to V_{BAT} from V_{DD} pin.

CHGEN	Data	Description
Write / Read	0	For non-re-chargeable battery use (default setting). SW2 is always OFF during V_{DD} drive, battery charging is not available.
	1	SW1, SW2 automatic controlled. For re-chargeable battery use

Table 35 CHGEN bit

In case of re-chargeable battery use, INIEN should be set to 1 to enable SW1, SW2 automatic control.

To stop charging the battery, CHGEN should be reset to 0.

2) INIEN bit

INIEN	Data	Description
Write / Read	0	I²C and FOUT operate even if the VDD terminal voltage is VDET1 or less. (Default) Make sure that the I²C interface does not reach at an undefined or intermediate voltage level. The power switching function is not operating in the 0 state due to power-on reset. Once this bit is set to 1 at least once, the power switching function will start operating. After activation, the power switching function continues to operate even if this bit is cleared back to zero.
	1	I²C, FOUT function is not available while $V_{DD} < V_{DET1}$. I²C, FOUT function is available while $V_{DD} > V_{DET1}$. CHGEN bit function is allowed to be enabled.

Table 36 INIEN bit

Note 1:

When used with power-on reset INIEN = 0, power switching is stopped and the power source is fixed to VDD-pin.

Therefore, it is recommended to set "INIEN = 1" at least once.

When the INIEN bit is set to 1, the power switching circuit is initialized and stabilized in the optimum state.

See "Initialization example".

Note 2:

When INIEN is set from 0 to 1 while $V_{DD} < V_{DET1}$, the I²C interface and the FOUT output are disabled immediately.

In this low-voltage condition, the I²C bus cannot be used to reset INIEN back to 0.

Therefore, when the supply voltage is below VDET1, INIEN must remain at 0 from power-on reset and should not be changed to 1.

Under this condition, the power-switching function remains stopped, and the power source stays fixed to the VDD pin.

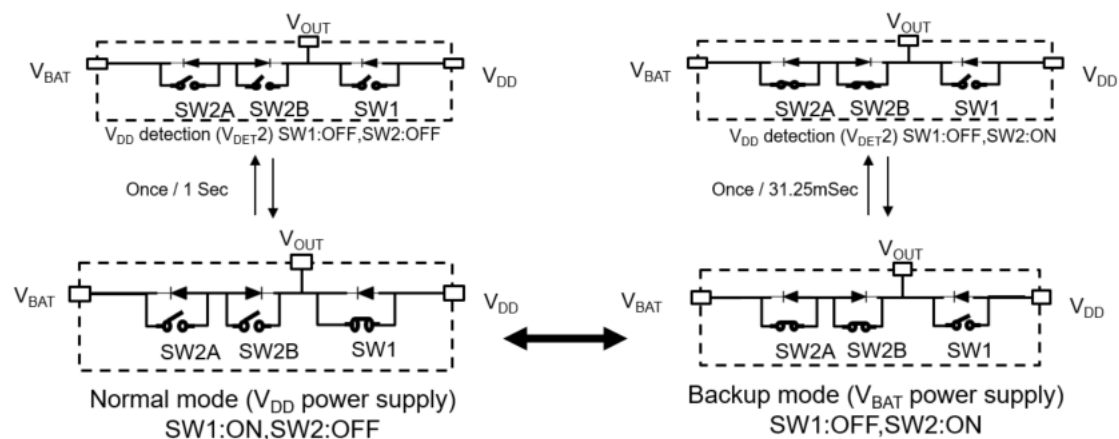


Figure 32 Non Re-chargeable battery SW1, SW2 control (INIEN = 1, CHGEN = 0)

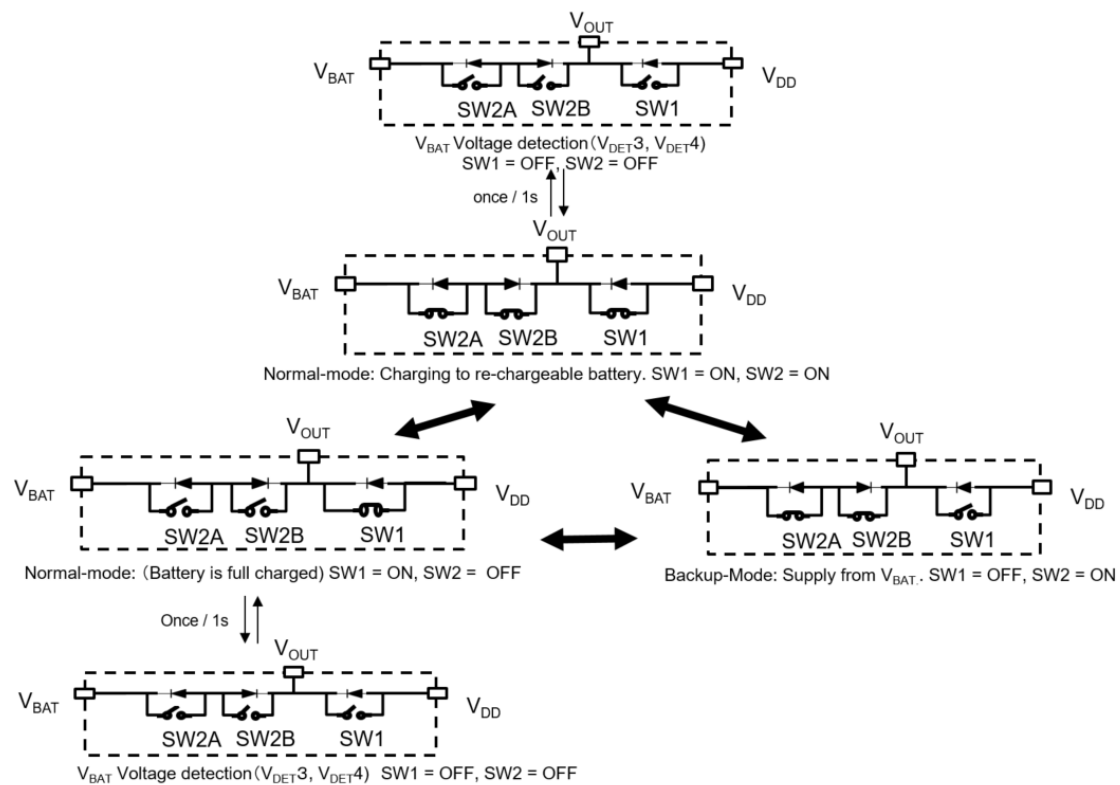


Figure 33 Re-chargeable battery SW1, SW2 control (INIEN = 1, CHGEN = 1)

Note:

In the normal mode without recharging function (CHGEN=0), SMPTSEL controls the SW1_Off duration once per second. (V_{DET2} always is detected. Periodic SW1_Off is used to prevent VOUT from buffering VDD.)

In the normal mode with recharging function (CHGEN=1), SMPTSEL controls both SW1_Off duration and SW2A&B_Off duration once per second. (V_{DET3} &4 are detected once per second. So, the detection of V_{DET3} &4 is in sync with $\overline{SW_Offs}$.)

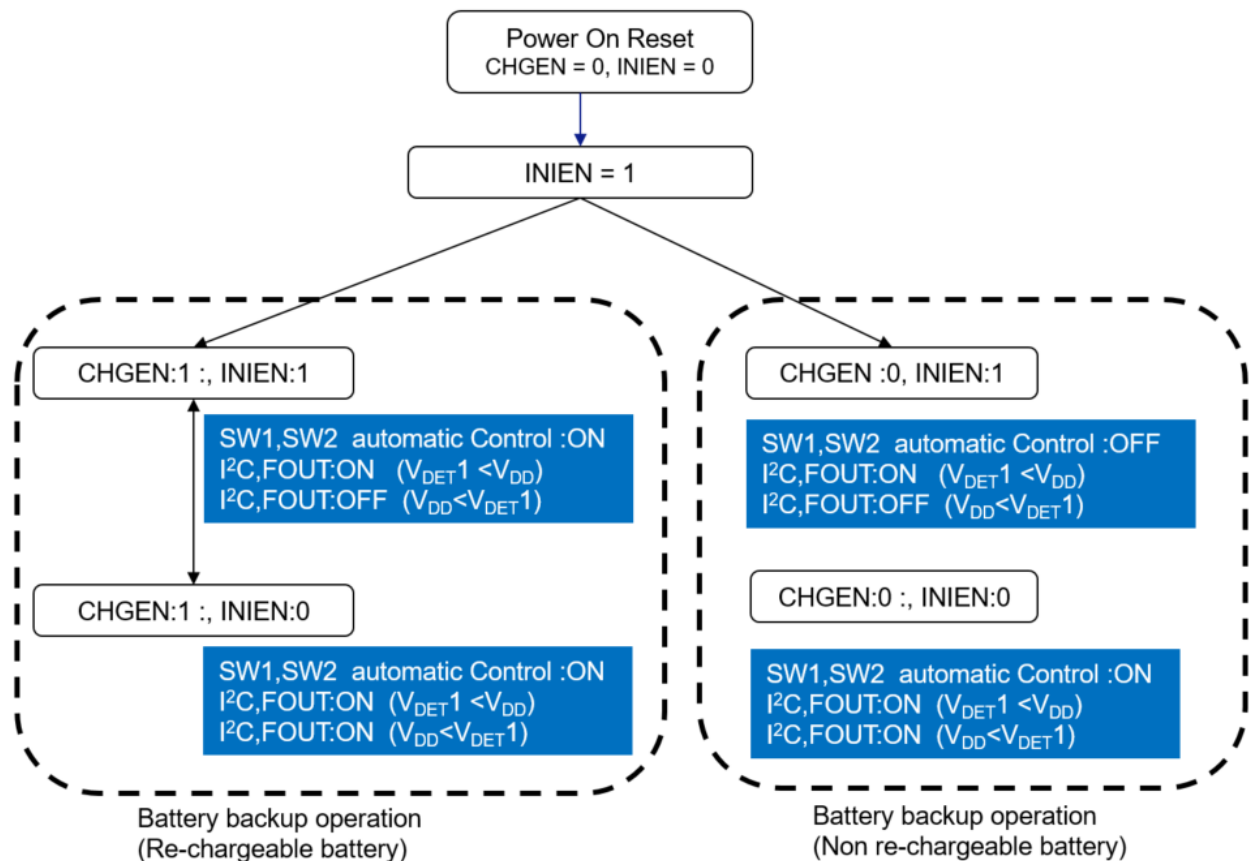


Figure 34 Battery backup (SW1, SW2 automatic control)

1) SMPTSEL1, SMPTSEL0 bit

- V_{DD} voltage detection: V_{DET1} (reset), V_{DET2} (voltage down):
Battery backup detection (V_{DET2}) operates constantly and SW1 is opened periodically for V_{DD} measurement.
During SW1: ON, external voltage to V_{DD} cannot be measured precisely because RTC internal voltage leaks to V_{DD} external voltage supply circuit even external circuit is power-down. In other words, the weaker power supply can be partially compensated by the leakage from V_{OUT} while SW1=ON, so the measured V_{DD} might be overestimated. Periodical SW1 = OFF makes disconnection between RTC internal voltage and external voltage supply, thus V_{DD} external voltage is measured precisely. V_{DD} external voltage dropping below V_{DET2} switches the power source of RTC to backup power.

See Figure 36 for V_{DD} detection (V_{DET2}) timing.

- V_{BAT} voltage detection: V_{DET3} (V_{BAT} full charge), V_{DET4} (V_{BAT} over discharge)
In case of normal mode, V_{BAT} voltage is precisely and periodically detected with condition of (SW1 OFF, SW2 OFF). The detection period is determined by combination of SMPTSEL1, SMPTSEL0. V_{BAT} will also potentially buffer the dropped V_{DD} while SW1&2 = ON. The longer SW1&2 OFF time could potentially shorten the buffering time of from V_{OUT} or V_{BAT} to the dropped V_{DD} . The length of SW1&2 Off can be shortened when the dropping speed of V_{DD} is fast (or the internal impedance of V_{DD} is lower).

See Figure 37 for V_{DET3} , V_{DET4} voltage detection timing.

(In case of CHGEN = 0, there is no charge operation SW2 = OFF)

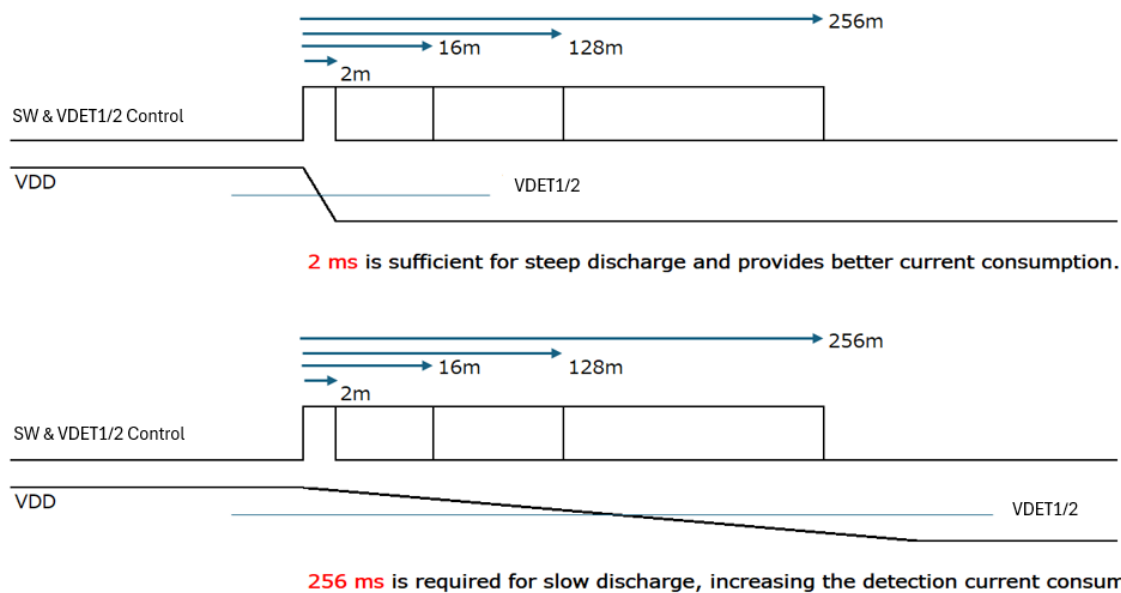
Power supply mode	Normal mode (Backup battery is charging)	Normal mode (Backup battery is fully charged)	Normal mode (After return from backup $V_{DET1} > V_{DD} > V_{DET2}$)	Backup mode
Reset detection $V_{DD} < V_{DET1}$	Constantly ON	Constantly ON	Constantly ON	Constantly OFF
Power switching detection $V_{DD} < V_{DET2}$	Constantly ON	Constantly ON	Constantly ON	Once/31.25 ms
Full charge detection $V_{BAT} > V_{DET3}$	Once/1.0 s	Once/1.0 s	Once/1.0 s	Constantly OFF
Low- V_{BAT} detection $V_{DD} < V_{DET4}$	Once/1.0 s	Once/1.0 s	Once/1.0 s	Constantly OFF

Table 37 Voltage detection timing

Power supply operation mode	SMPTSEL1,0	VDD operation (Backup battery is charging)	VDD operation (Backup battery is fully charged)	VDD operation (After return from backup $V_{DET1} > V_{DD} > V_{DET2}$)
SW1 Off time. *	00b (default)	2 ms	2 ms	2 ms
	01b	16 ms	16 ms	2 ms
	10b	128 ms	128 ms	2 ms
	11b	256 ms	256 ms	2 ms

* In normal mode, when operating the RTC on VDD-supply, SW1 has to be opened (Off) to precisely perform the V_{DD} voltage detection for below mentioned times. The timing of OFF at SW1 and SW2AB is in sync with the same second counter.

Table 38 VDET3, VDET4 intermittent detection period

Figure 35 V_{DD} detection (V_{DET2}) timing

V_{DD} voltage drop detection (V_{DET2}) is work always, in Normal mode.

A shorter SW1:OFF time is suitable for detecting fast voltage drops on V_{DD} because the lower supply impedance allows the capacitor at V_{OUT} to discharge more quickly. Conversely, slower voltage drops – typically associated with a higher internal supply impedance – require a longer SW1:OFF time for reliable detection. However, increasing the SW1:OFF duration also raises current consumption.

Users are requested to evaluate SW1:OFF period based on the actual system configuration and characteristics.

In backup mode V_{DD} detection (V_{DET2}) is activated once every 31.25 ms.

Note: Re-chargeable battery is charged through diode during the term of SW1 = OFF. Longer this term (ex. 256 ms) makes decreasing battery charging efficiency.

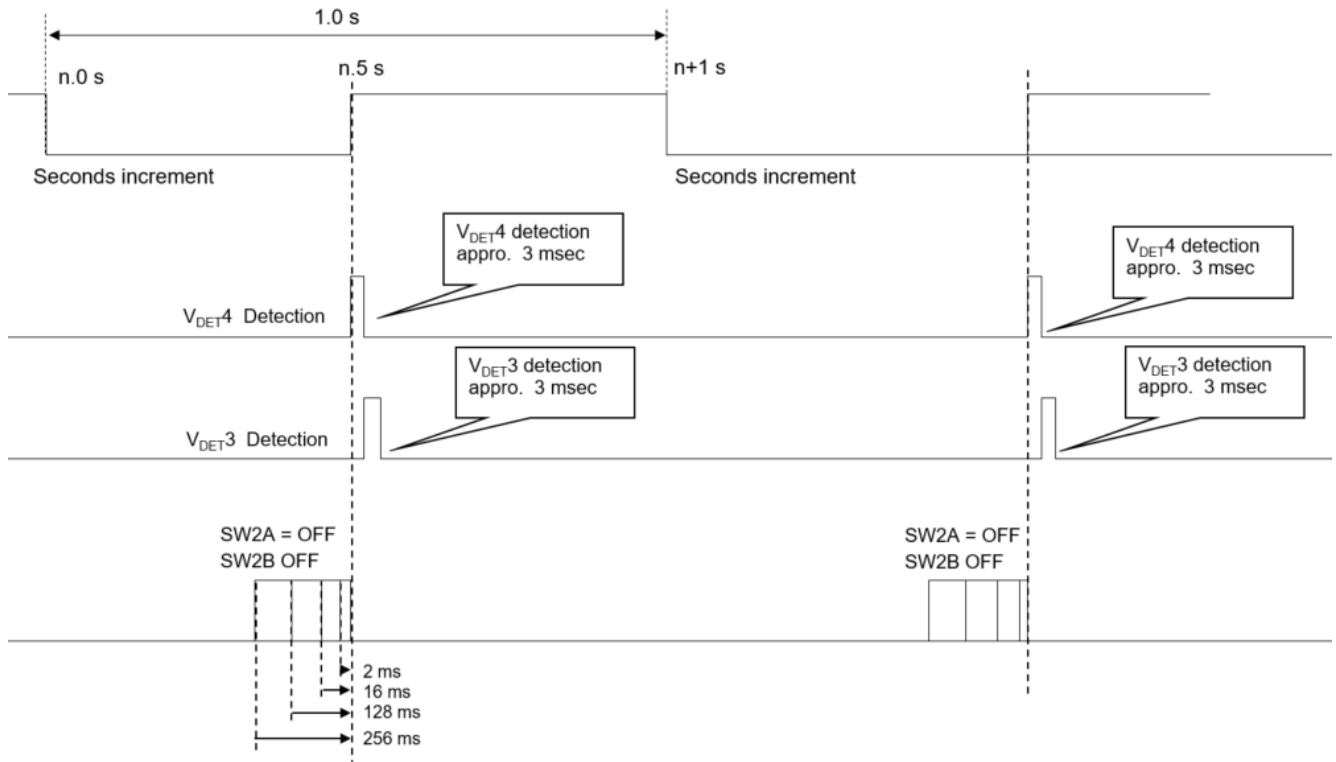


Figure 36 VDET3, VDET4 voltage detection timing) BFBVSEL1, BFBVSEL0 bit

15.6. Detection voltage setting

	Item	Symbol	Detect voltage Typ.	setting
VDET1	Reset /Reset-release voltage	+VDET11 / - VDET11	2.8V / 2.75V	RSVSEL = 0 (default)
		+VDET12 / - VDET12	2.7V / 2.65V	RSVSEL = 1
VDET2	Backup switchover/recover voltage	+VDET2 / - VDET2	1.35V / 1.30V	
VDET3	Full charge detection voltage	+VDET31 / - VDET31	3.02V / 2.97V	BFBVSEL = 00b (default)
		+VDET30 / - VDET30	2.92V / 2.87V	BFBVSEL = 01b
		+VDET32 / - VDET32	3.08V / 3.03V	BFBVSEL = 10b
VDET4	V _{BAT} low-voltage detection voltage	-VDET4	2.4V	

Table 39 VDET1, VDET2, VDET3, VDET4 Setting

- 1) The full-charge detection (VDET3) and low- V_{BAT} detection (VDET4) control SW2.

BFVSEL1	BFVSEL0	Description
0	0	3.02 V (default)
0	1	3.08 V
1	0	2.92 V
1	1	OFF (Charging without limit)

Table 40 BFVSEL1, BFVSEL0

- 2) VBFF bit

This bit indicates if the battery is fully charged (update Every 1sec)

VBFF	Data	Description
Read	0	Charging
	1	Full charge of V_{BAT} detected (voltage level defined by BFVSEL-bit is reached)

This flag shows the V_{BAT} charge state.

Table 41 VBFF

- 3) VBLF bit

The flag of Low V_{BAT} detection ($V_{BAT} < V_{DET4}$)

VBLF	Data	Description
Write	0	Cleared to zero to prepare for the next status detection.
	1	Invalid (writing a 1 will be ignored)
Read	0	—
	1	Low- V_{BAT} has been detected (V_{DET4})

Table 42 VBLF

- 4) VBLFE bit

Enable/Disable for the battery Low detection (Every 1 s).

VBLFE	Data	Description
Write	0	CHGEN:0 VBLF detection not available CHGEN:1 VBLF detection available (during normal mode and re-chargeable battery charging)
	1	VBLF detection is available during V_{DD} supply.

Table 43 VBLFE

To use VBLF (V_{BAT} Low Flag) detection, the device must first have INIEN = 1 set at least once. After initialization, enable the VBLFE bit to activate the VBLF detection function. During the normal mode (VDD-powered operation), the device can detect V_{BAT} low-voltage conditions for both non-rechargeable and rechargeable batteries.

To enable the VBLF function either:

When the VBAT charge function is enabled (CHGEN = 1, VBLFE=0 or 1) and the RTC is in normal mode. (For secondary battery), or

When VDD is available and VBLFE=1, meaning whenever the RTC is operating in normal mode. (For primary battery).

However, in backup mode, the VBLF function is not active. V_{BAT} low voltage will only be detected after the device returns to normal mode, at which point VBLF detection resumes.

8) STOP bit function

When STOP = 1, the periodic 31.25 ms V_{DET2} detection is disabled during backup mode. As a result, power-supply switchover may not operate properly, which can lead to potential leakage current.

Therefore, if the device enters backup mode while STOP = 1, the STOP bit must be cleared to 0 immediately after VDD is restored to ensure proper operation.

15.7. Power supply control

By setting battery backup registers (INIEN, CHGEN), the JR8310 operates like following either in re-chargeable battery or non-re-chargeable battery operation.

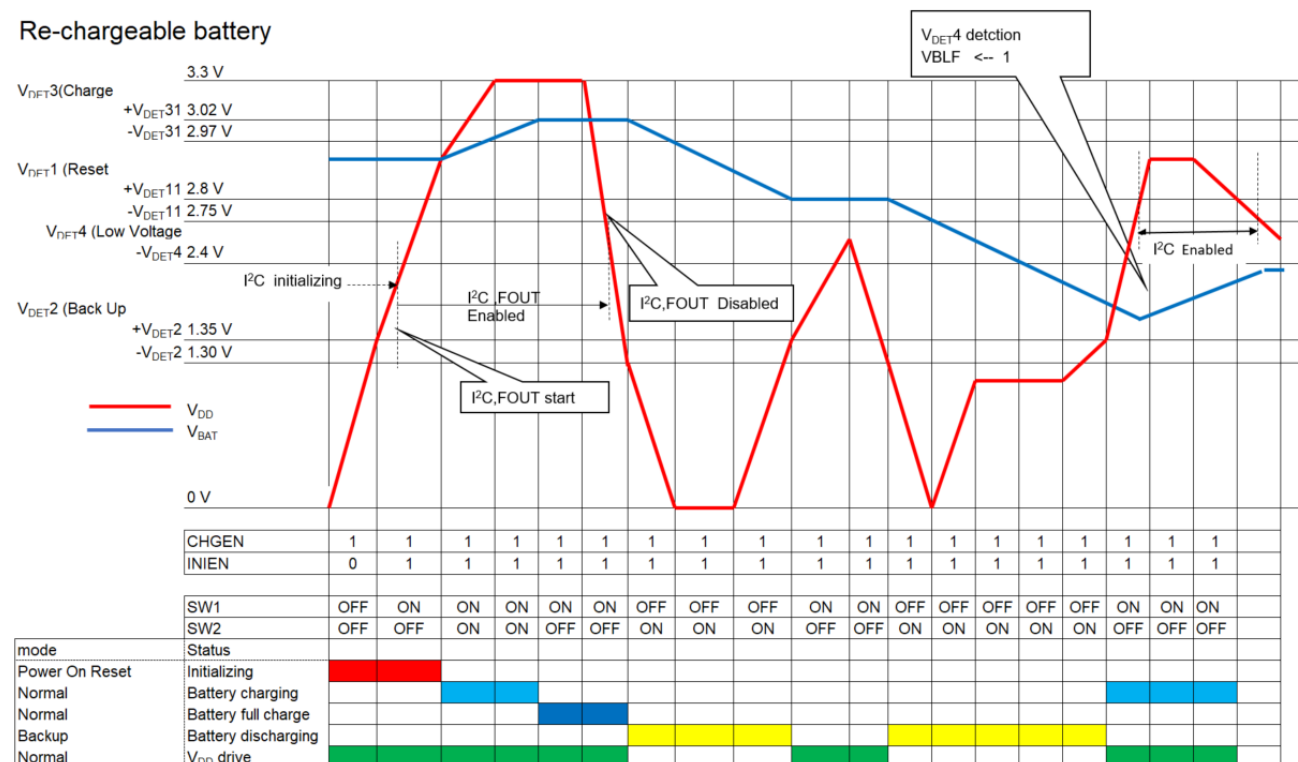


Figure 37 Re-chargeable battery operation

Non Re-chargeable battery

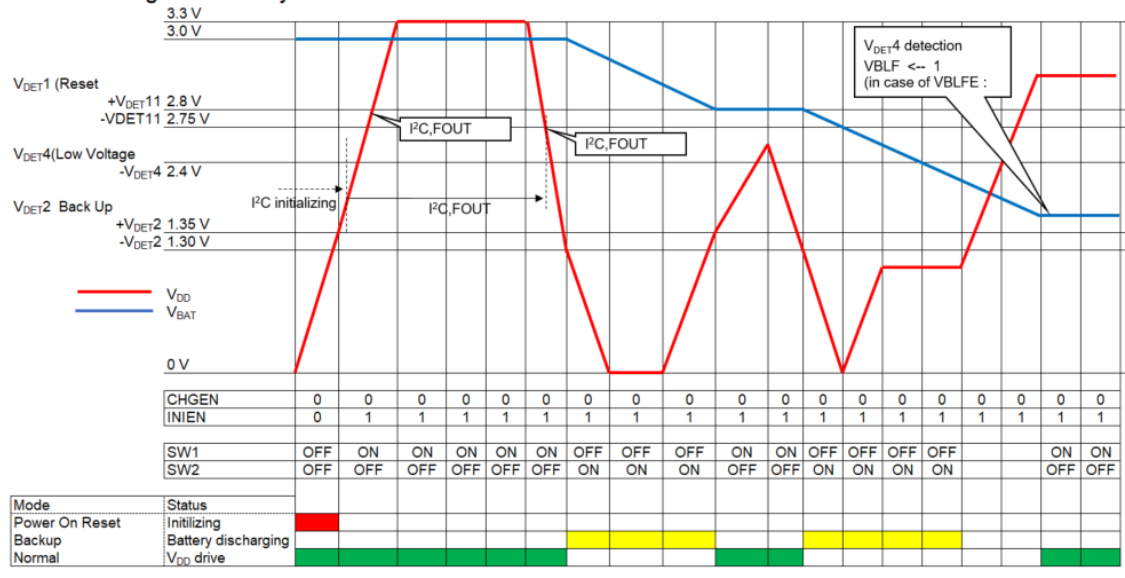
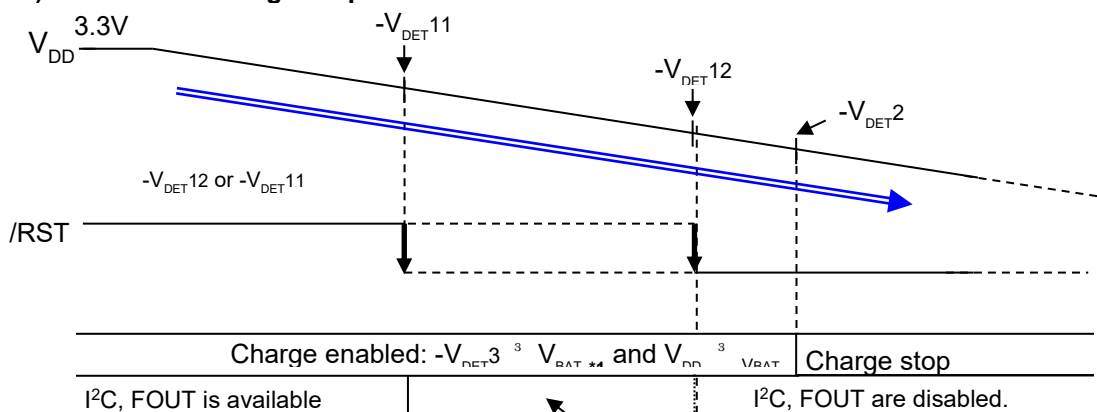


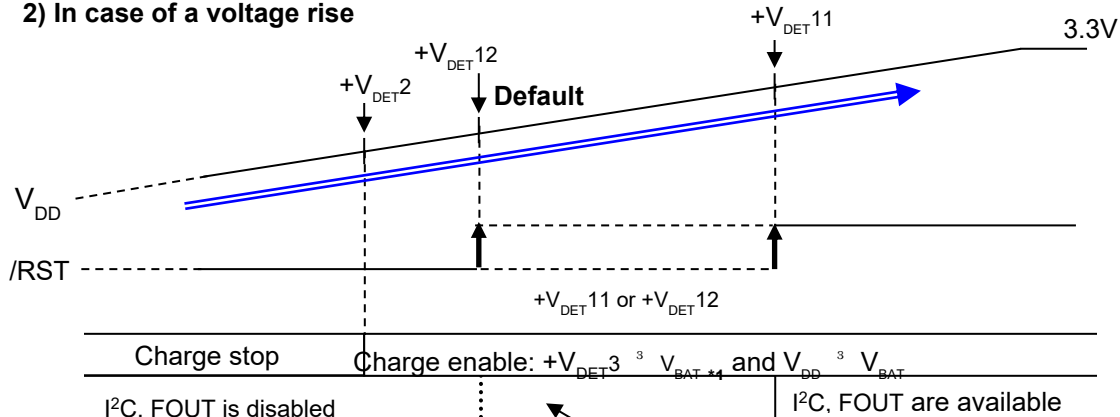
Figure 38 Non re-chargeable battery operation

15.8. Main power supply (V_{DD}) voltage and operation state (INIEN bit = 1)

1) In case of a voltage drop

A function of I²C and FOUT stops in sync with the

2) In case of a voltage rise

A function of I²C and FOUT stops in sync with the /RST output*When full charge detection was deactivated (V_{DET3}) by register setting, V_{BAT} is only charged if $V_{DD} > V_{BAT}$ Figure 39 I²C, FOUT operation during voltage drop and rise

15.9. Backup power supply (V_{BAT}) voltage and a charge state

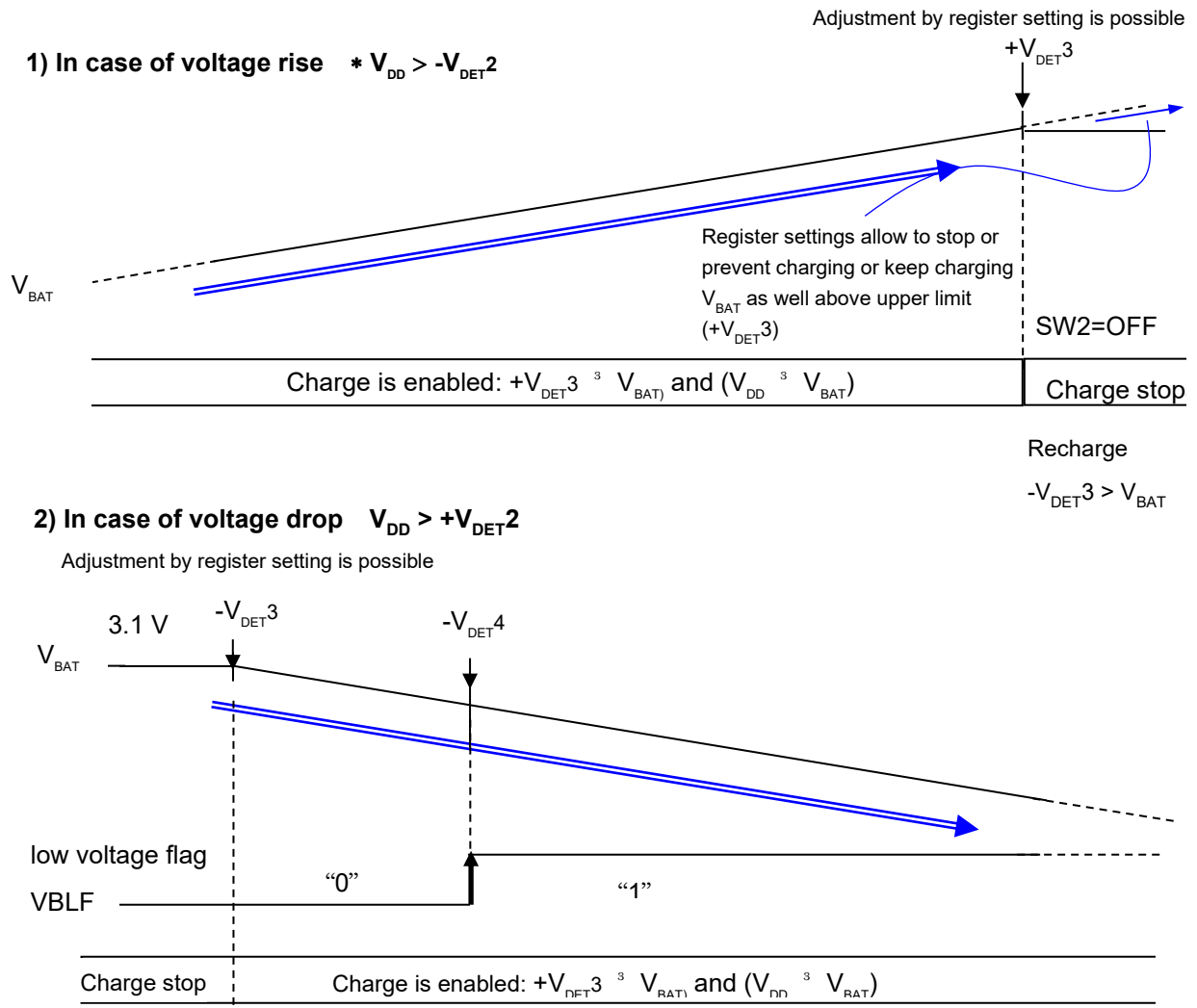


Figure 40 Re-chargeable battery operation during voltage rise and down

While $V_{BAT} > +V_{DET3}$, there are three options of operation:

1. Stop charging (Retain CHGEN = 1 then the charging stops if $V_{BAT} > +V_{DET3}$)
If CHGEN = 1 and $V_{DD} > V_{BAT}$, the charge goes on till V_{BAT} reaches $+V_{DET3}$ level. The level of V_{DET3} can be set with BFMSEL0/1 bits.
2. Prevent charging (Reset CHGEN from 1 to 0)
CHGEN = 0 disables the charge function even if $V_{BAT} < +V_{DET3}$
3. Keep charging even if $V_{BAT} > +V_{DET3}$
This option would be enabled if BFMSEL0/1 is set to 1/1

The recharging starts while $V_{BAT} < -V_{DET3}$ and $V_{DD} > V_{BAT}$.

When the discharging rate of V_{BAT} is higher than the charging rate, the V_{BAT} definitely will go downwards.

For $V_{BAT} < -V_{DET4}$, the charging can still work but only the flag of VBLF be set to 1.

16. Reset output function

This RTC has a built-in Reset-Controller, which outputs a Reset-signal on the /RST-pin to control external HW like MCUs in case of a drop in supply voltage. When the VDD voltage drops below V_{DET1} (register selectable V_{DET11} or V_{DET12}), a /RST-signal is output. Once V_{DD} rises beyond V_{DET1} voltage again, the /RST-signal is released.

In case INIEN bit is set to "1", I²C and FOUT are stopped when V_{DD} drops below V_{DET1} .

Related register of reset output function

Address h	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
1D	Flag Register	VBLF	0	UF	TF	AF	RSF	VLF	VBFF
1F	Control Register1	SMP TSEL 1	SMP TSEL0	CHG EN	INIEN	0	RS VSEL	BF VSEL1	BF VSEL 0

1) RSVSEL-bit

Setting of V_{DET1} voltage level. In case V_{DD} drops below this level, the /RST-signal is output and the I/F and FOUT output are stopped (depending on INIEN-bit setting).

RSVSEL	Data	Description
Write / Read	0	-VDET11 (2.75 V) (default)
	1	-VDET12 (2.70 V)

Table 44 RSVSEL

2) RSF-bit

This bit holds the result of detecting the reset voltage.

RSF	Data	Description
Write	0	The RSF is cleared to 0 and waiting for next low voltage detection.
	1	Invalid (writing a 1 will be ignored)
Read	0	-
	1	A voltage drops below $-V_{DET1}$ was detected.

Table 45 RSF bit

17. Digital offset function

With this function it is possible to increase or decrease the speed of the time counting and thus put a positive or negative offset to the clock precision. The adjustment range for this offset correction is $+192.3 \times 10^{-6}$ to -195.3×10^{-6} in steps of 3.05×10^{-6} .

17.1. Digital offset register

Address h	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
30	Digital offset	DTE	L7	L6	L5	L4	L3	L2	L1

- DTE="1" enables the digital offset function.
When the digital offset function is enabled, the digital offset register digitally offsets the sub-second clocks according to the values set in the digital offset register. This correction of the second time register occurs every 10 seconds and the level of correction depends on the offset required. When outputting a 32.768 kHz signal on FOUT-pin, this function has no influence, since the oscillation frequency of the built-in crystal does not change by using this function. In case of outputting a 1 Hz or 1024 Hz signal on FOUT, the offset correction will cause a certain jitter on the clock signal. Alarm function as well as the Wakeup Timer function (if source clock slower than 4096 Hz is selected) are affected by this function.
- In order to disable the digital offset function, set to DTE = "0". In this case the L1 to L7 are ignored.
- Below table shows the relationship of the L7~L1 bit and the digital offset value
When the L7 bit = "0", the offset is positive (clock runs faster), when the L7 bit = "1", the offset is negative (the clock runs slower).

Digital offset bits							Offset value ($\times 10^{-6}$)
L7	L6	L5	L4	L3	L2	L1	
0	1	1	1	1	1	1	+192.2 6
0	1	1	1	1	1	0	+189.2 1
•							•
•							•
0	0	0	0	0	1	0	+6.10
0	0	0	0	0	0	1	+3.05
0	0	0	0	0	0	0	±0.00
1	1	1	1	1	1	1	-3.05
1	1	1	1	1	1	0	-6.10
•							•
•							•
1	0	0	0	0	0	1	-192.2 6
1	0	0	0	0	0	0	-195.3 1

Table 46 Digital Adjustment

The offset value is calculated on basis of a shift of the built-in crystal frequency.

- How to calculate the offset value
 - 1) When the offset value is positive:
 $L[7 \sim 1] = [\text{Offset Value}] / 3.05$ However, decimals are discarded.
 Example calculation: When the offset value is $+192 \times 10^{-6}$
 $L[7 \sim 1] = 192.26 / 3.05 = 63 \text{ (Dec)}$
 $= 0111111(\text{bin})$ is set.
 - 2) When the offset value is negative:
 $L[7 \sim 1] = 128 - [\text{Offset Value}] / 3.05$ However, decimals are discarded.
 Example calculation: When the offset value is -158×10^{-6}
 $L[7 \sim 1] = 128 - (158 / 3.05) = 76 \text{ (Dec)} = 1001100(\text{bin})$ is set.
 - 3) When calculate from accuracy of a clock
 To adjust 30 seconds in 30 days:
 Example calculation: $30\text{sec.} / 2592000\text{s (30days)} = 11.57 \times 10^{-6}$

 Positive offset
 $L[7 \sim 1] = 11.57 / 3.05 = 4 \text{ (Dec)}$ However, decimals are discarded.
 $= 0000100(\text{bin})$ is set.

 Negative offset
 $L[7 \sim 1] = 128 - (11.57 / 3.05) = 124 \text{ (Dec)}$ However, decimals are discarded.
 $= 1111100(\text{bin})$ is set.

17.2. Effect of the digital offset function to other functions

Because this function adjusts an internal sub-second clock, this function affects the Wakeup timer interrupt function and FOUT function

1) FOUT function

- 1 Hz setting: Once in 10 seconds, the 1 Hz period fluctuates.
- 1024 Hz setting: Once in 10 seconds, the 1024 Hz period fluctuates.
- *There are cases where there is no fluctuation, depending on the offset correction value.
- 32.768 kHz Not affected.

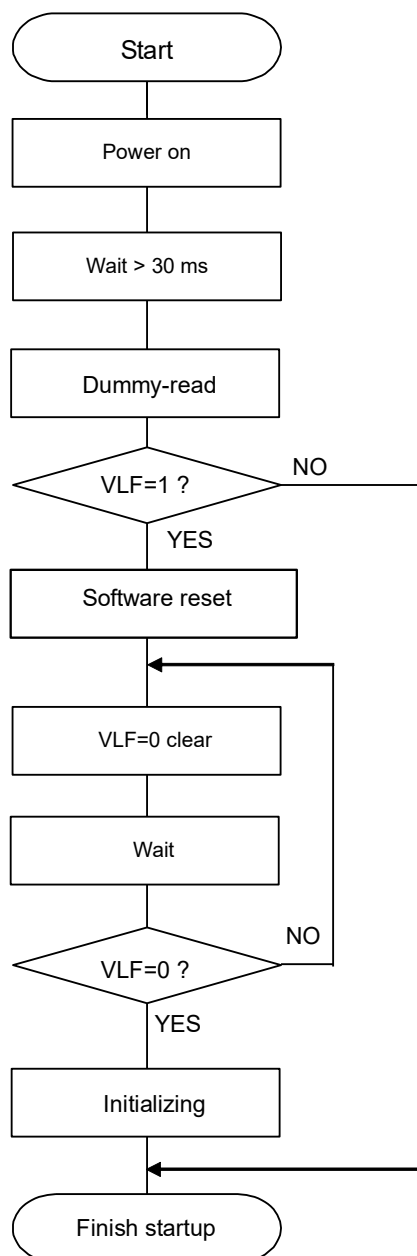
2) Wakeup timer interrupt function

- 64 Hz or 1 Hz source clock setting: Once in 10 seconds, the period fluctuates.
 When the timer intervals are long, the fluctuations appear small.
- 4096 Hz source clock setting: Not affected.

18. Flow-chart

The following flow-chart is one example, but it is not necessarily applicable for every use-case and not necessarily the most effective process for individual applications.

18.1 Initializing example



- At least 30 ms wait time is needed. So that it is stable RTC. 40 ms is not oscillation startup time

- When the power supply conditions for which Power-On Reset is executed cannot be satisfied, then must be execute a Dummy-read.

Dummy read is one time read access to a free address
Ignore ACK / NACK from RX8130CE in Dummy-read.

Judge RX8130CE returned from backup normally, or fail.

When the power conditions for which the power-on reset is executed are not satisfied, execute a software reset.
For [Software Reset], start from "4) of "18.2 Software Reset."

VLF cannot be cleared to 0 until internal oscillation starts. ·

Set any waiting time.

Set the maximum number of loops, for an trouble of crystal oscillation

Figure 41 Example flow (Power initialization)

18.2 Software Reset

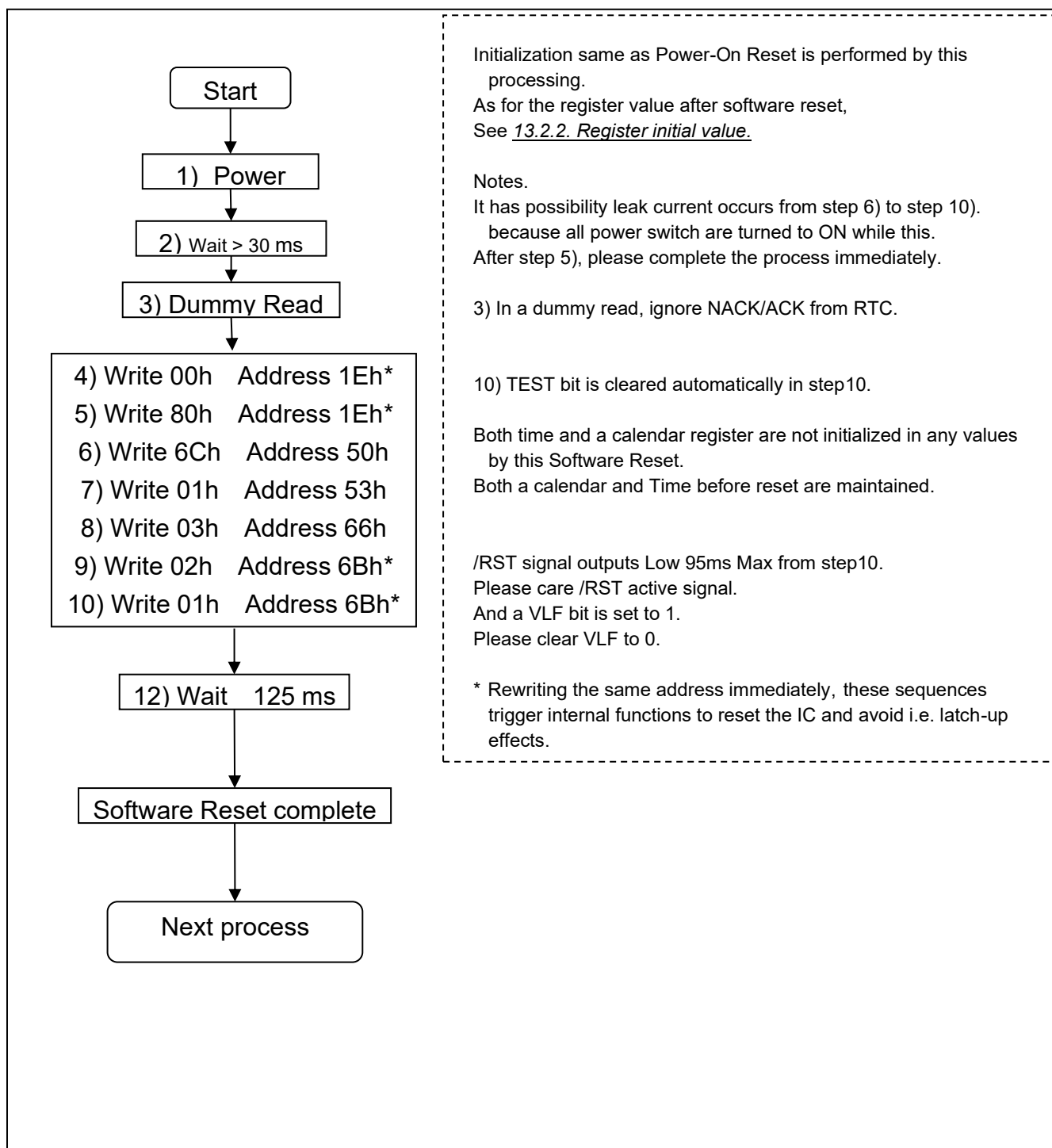


Figure 42 Example Flow (Software Reset)

18.3 Example of Initialization routine

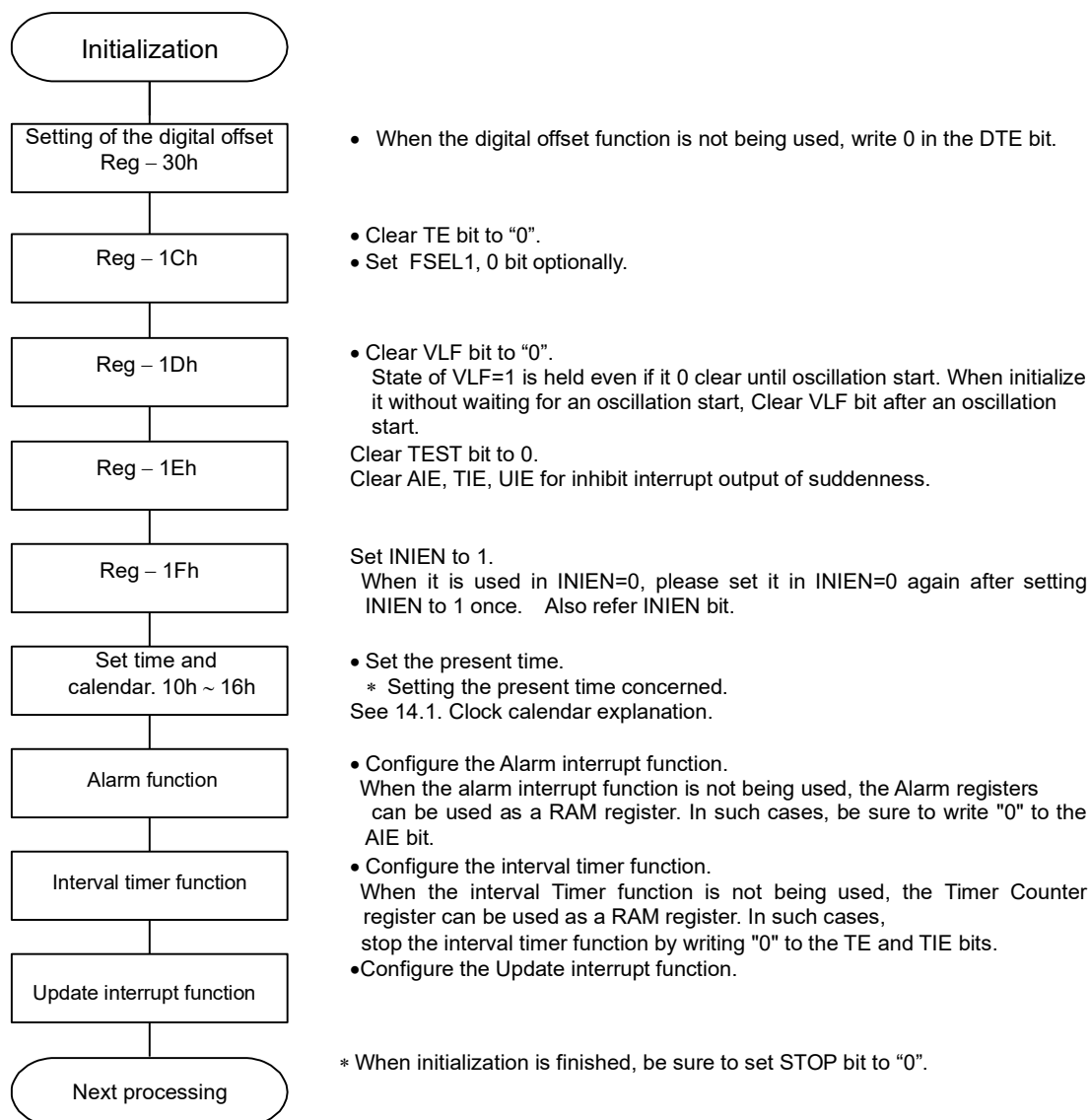


Figure 43 Example flow (Initialization)

18.4 Example of Initialization routine (only clock usage)

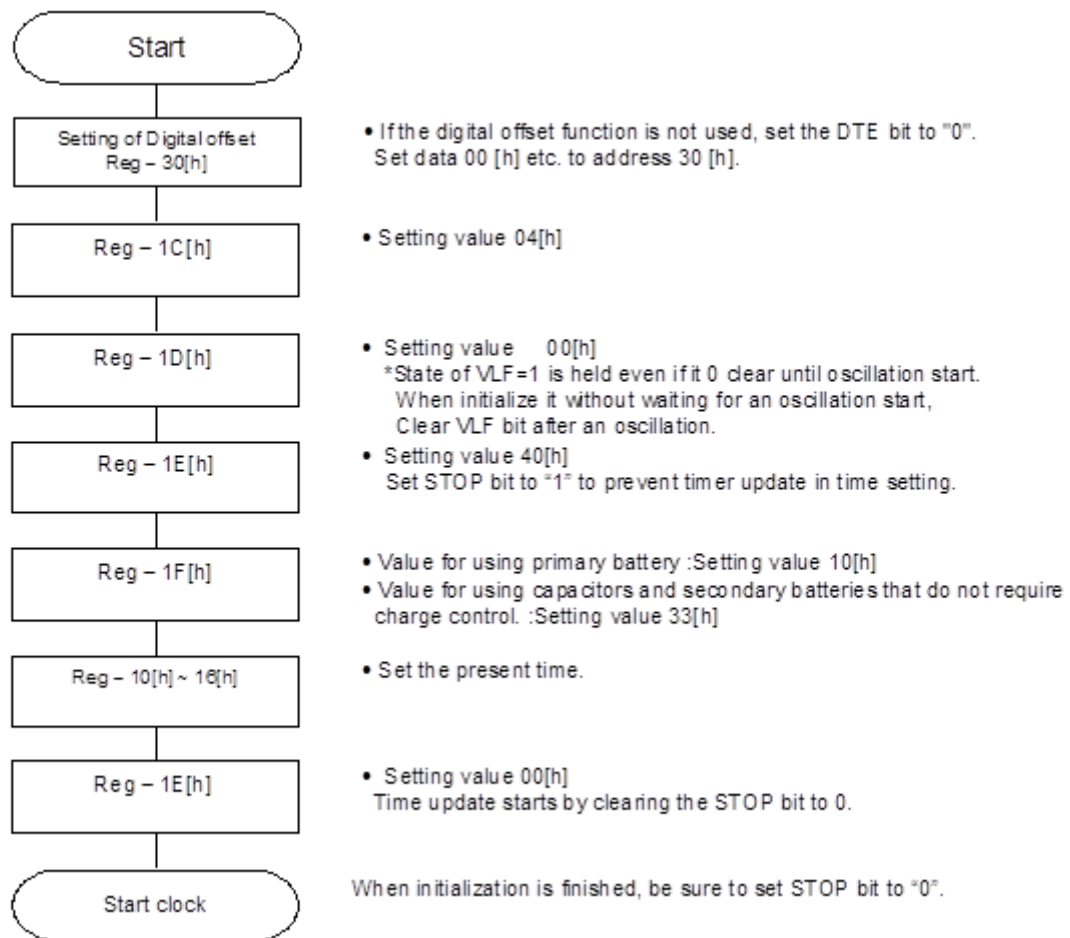


Figure 44 Example flow (initialization only clock usage)

18.5 The setting of the clock and calendar

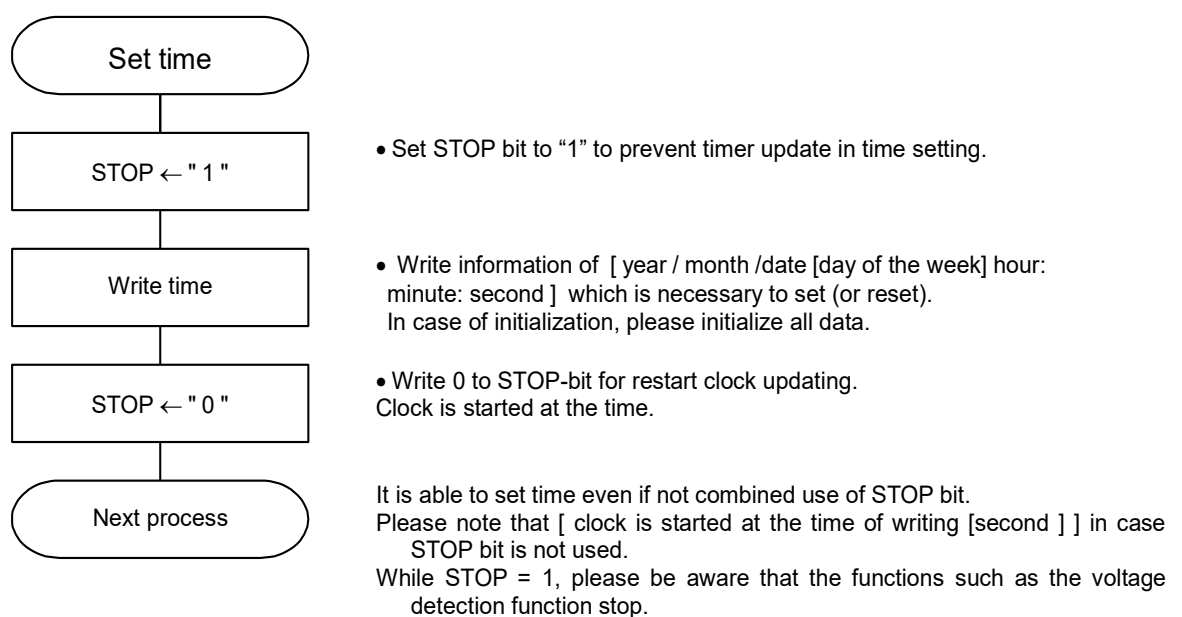


Figure 45 Example flow (Clock, calendar setting)

18.6 The reading of the clock and calendar

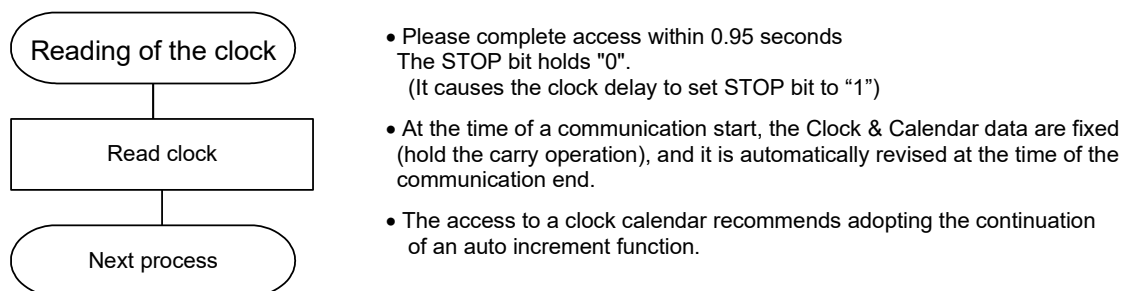


Figure 46 Example flow (Clock, calendar reading)

18.7 Setting example of the wakeup timer interrupt function

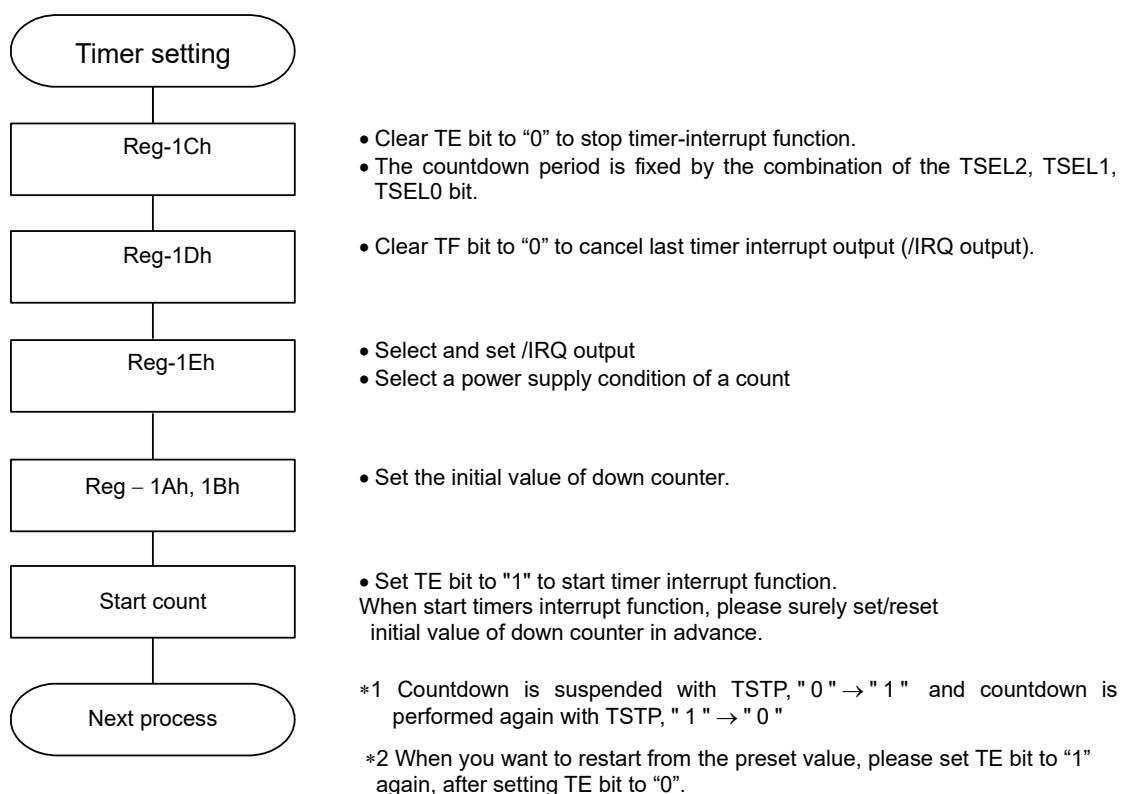


Figure 47 Example flow (Wakeup timer interruption)

18.8 Setting example of the Alarm interrupt function

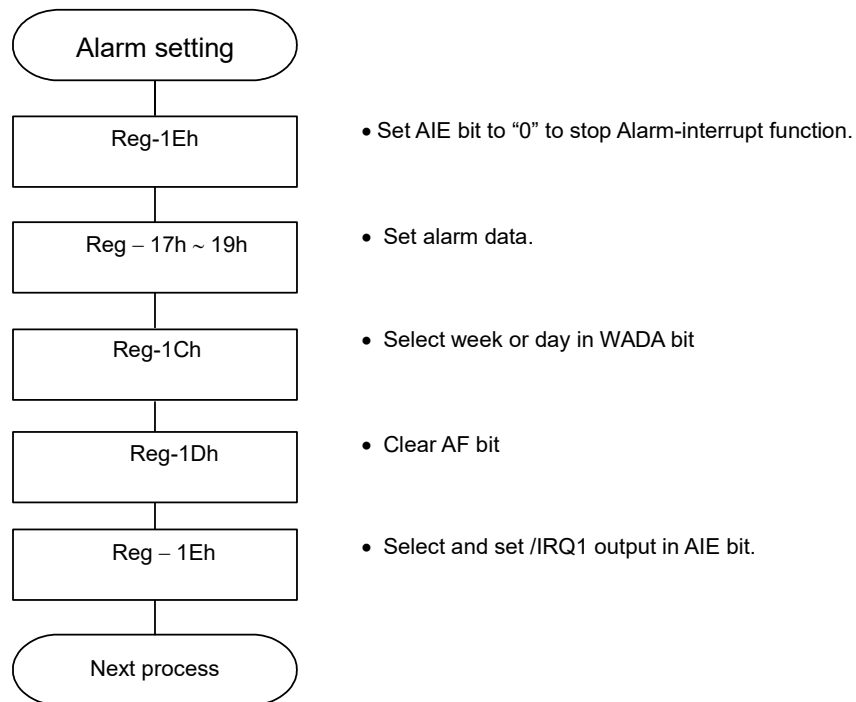


Figure 48 Example flow (Alarm interruption)

19 Serial communication

19.1 Overview of I²C-Bus Interface

The I²C-bus supports bi-directional communications via two signal lines: the SDA (data) line and SCL (clock) line. A combination of these two signals is used to transmit and receive communication start/stop signals, data transfer signals, acknowledge signals, and so on.

Both the SCL and SDA signals are held at High level whenever communications are idled. The starting and stopping of communications is controlled at the rising edge or falling edge of SDA while SCL is at high level.

19.2 Data transfers

Data transfers are performed in 8-bit (1 byte) units once the START condition has occurred. There is no limit on the amount (bytes) of data that are transferred between the START condition and STOP condition.
(However, the transfer time must be no longer than 0.95 seconds.)

19.3 Starting and stopping I²C-Bus communications

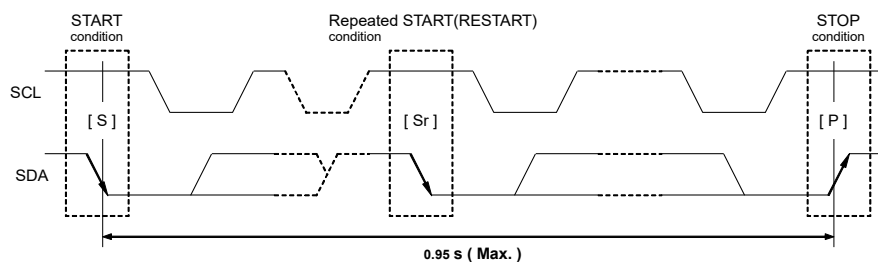


Figure 49 I²C-Bus start/stop timing

1) START condition, repeated START condition, and STOP condition

(1) START condition

- The SDA level changes from high to low while SCL is at high level.

(2) STOP condition

- This condition regulates how communications on the I²C-Bus are terminated.

The SDA level changes from low to high while SCL is at high level.

(3) Repeated START condition (RESTART condition)

- In some cases, the START condition occurs between a previous START condition and the next STOP condition, in which case the second START condition is distinguished as a RESTART condition. Since the required status is the same as for the START condition, the SDA level changes from high to low while SCL is at high level.
- When accessing this device, all communication from transmitting the start condition to transmitting the stop condition after access should be completed within 0.95 seconds. If communication requires 0.95 seconds or longer, the I²C bus interface would be reset by the internal bus timeout function.

19.4 Slave address

The I²C-Bus devices do not have any chip select or chip enable pins. All I²C-Bus devices are memorized with a fixed unique number in it. The chip selection on the I²C-Bus is executed, when the interface starts, the master device sends the required slave address to all devices on the I²C-Bus. The receiving device only reacts for interfacing, when the required slave address is agreed with its own slave address.

During the actual data transmission, the transmitted data contains the slave address and the bit determined by R/W function.

Slave address							R/W bit
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	1	1	0	0	1	0	R/W
0 is Write mode 1 is Read mode							↑

19.5 System configuration

All ports connected to the I²C-Bus must be either open-drain or open-collector ports in order to enable AND connect to multiple devices.

SCL and SDA are both connected to the VIO line via a pull-up resistance. Consequently, SCL and SDA are both held at high level when the bus is released (when communication is idled).

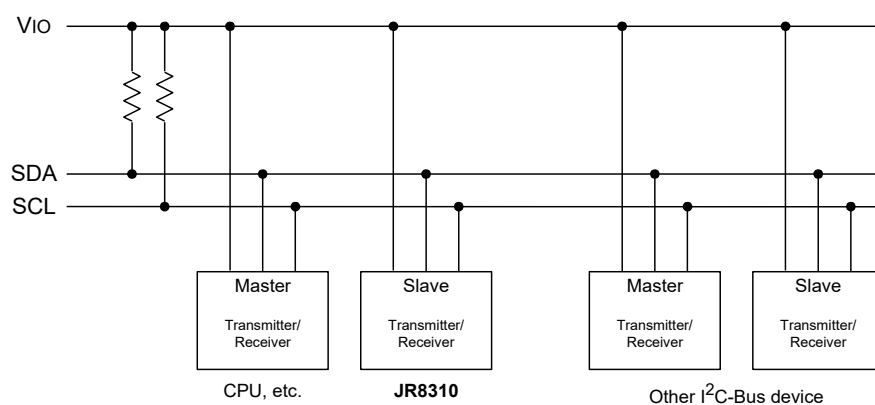


Figure 50 I²C-Bus connection

Any device that controls the data transmission and data reception is defined as a "Master". and any device that is controlled by a master device is defined as a "Slave". The device transmitting data is defined as a "Transmitter" and the device receiving data is defined as a receiver"

In the case of this RTC module, controllers such as CPU or MCU are defined as master devices and the RTC module is defined as a slave device. When a device is used for both transmitting and receiving data, it is defined as either a transmitter or receiver depending on the conditions.

19.6 I²C-Bus protocol

In the following sequence descriptions, it is assumed that the CPU/MCU is the master and the JR8130 is the slave.

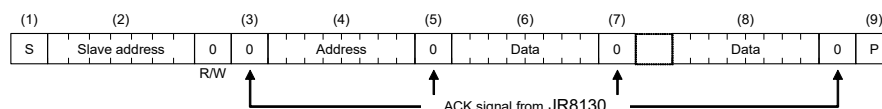
1) Address specification write sequence

Since the JR8130 includes an address auto increment function, once the initial address has been specified, the JR8130 increments (by one byte) the receive address each time data is transferred.

Address circulation of auto increment function.	10h -> 1Fh -> 10h
	20h -> 2Fh* -> 20h
	30h -> 3Fh** -> 30h

Note: *Only accessing 20h ~ 23h / **Only accessing to 30h and 31h

- (1) CPU/MCU transfers start condition [S].
- (2) CPU/MCU transmits the JR8130 's slave address with the R/W bit set to write mode.
- (3) Check for ACK signal from JR8130.
- (4) CPU/MCU transmits write address to JR8130.
- (5) Check for ACK signal from JR8130.
- (6) CPU/MCU transfers write data to the address specified at (4) above.
- (7) Check for ACK signal from JR8130.
- (8) Repeat (6) and (7) if necessary. Addresses are automatically incremented.
- (9) CPU/MCU transfers stop condition [P].

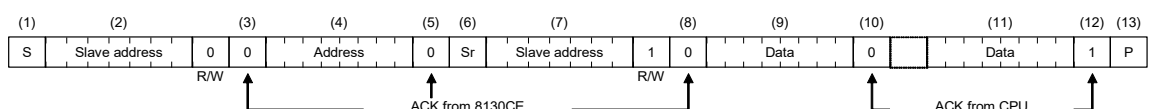


3) Address specification read sequence

After using write mode to write the address to be read, set read mode to read the actual data.

- (1) CPU/MCU transfers start condition [S].
- (2) CPU/MCU transmits the JR8130's slave address with the R/W bit set to write mode.
- (3) Check for ACK signal from JR8130.
- (4) CPU/MCU transfers address for reading from JR8130.
- (5) Check for ACK signal from JR8130.
- (6) CPU/MCU transfers RESTART condition [Sr] (in which case, CPU/MCU does not transfer a STOP condition [P]).

- (7) CPU/MCU transfers JR8130's slave address with the R/W bit set to read mode.
- (8) Check for ACK signal from JR8130 (from this point on, the CPU/MCU is the receiver and the JR8130 is the transmitter).
- (9) Data from address specified at (4) above is output by the JR8130.
- (10) CPU/MCU transfers ACK signal to JR8130.
- (11) Repeat (9) and (10) if necessary. Read addresses are automatically incremented.
- (12) CPU/MCU transfers ACK signal for "1".
- (13) CPU/MCU transfers stop condition [P].



4) Read sequence when address is not specified

Once read mode has been initially set, data can be read immediately. In such cases, the address for each read operation is the previously accessed address + 1.

- (1) CPU/MCU transfers start condition [S].
- (2) CPU/MCU transmits the JR8130's slave address with the R/W bit set to read mode.
- (3) Check for ACK signal from JR8130 (from this point on, the CPU/MCU is the receiver and the JR8130 is the transmitter).
- (4) Data is output from the JR8130 to the address following the end of the previously accessed address.
- (5) CPU/MCU transfers ACK signal to JR8130.
- (6) Repeat (4) and (5) if necessary. Read addresses are automatically incremented in the JR8130.
- (7) CPU/MCU transfers ACK signal for "1".
- (8) CPU/MCU transfers stop condition [P].

20 Circuit Diagram connection

20.1 Typical MCU connection

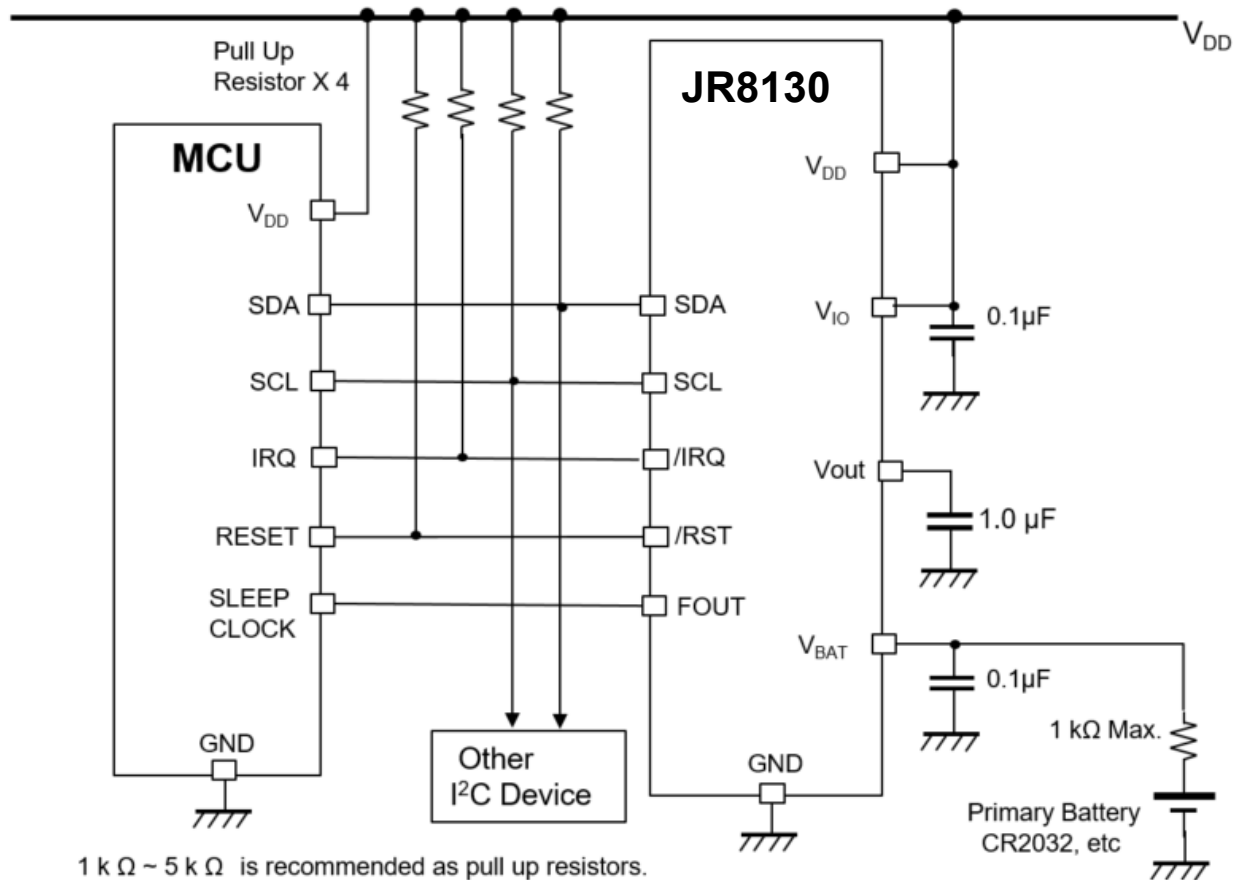
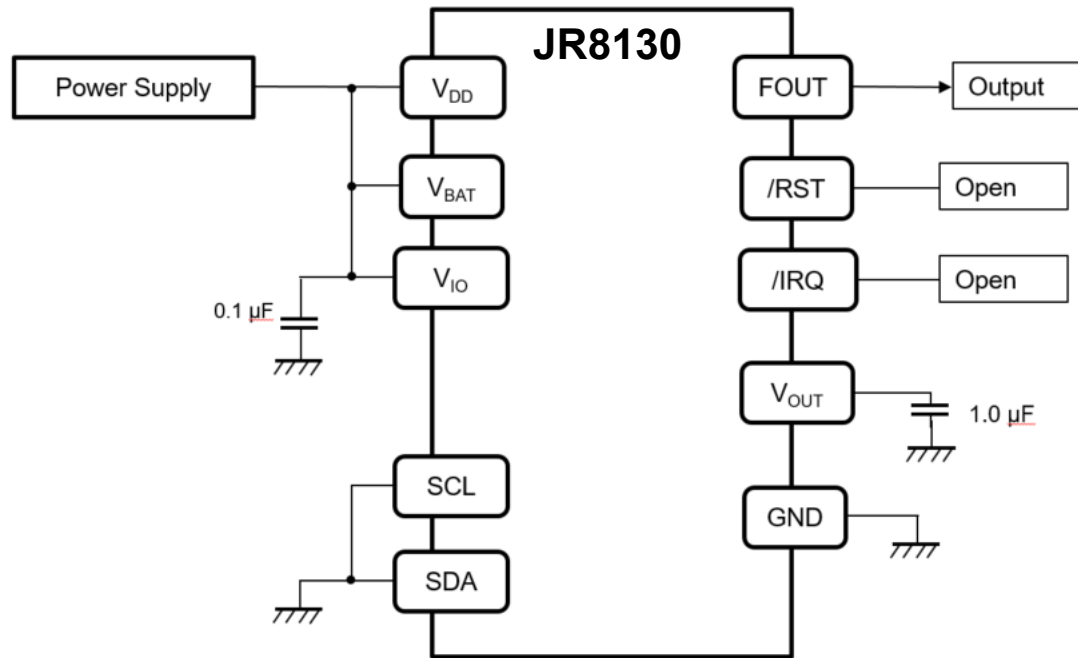


Figure 51 Typical MCU connection

20.2 32.768 kHz oscillator application connection

See also [14.6.FOUT function](#)



Each capacitor should be located in the vicinity of RTC pins.

Figure 52 32.768 kHz oscillator connection

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