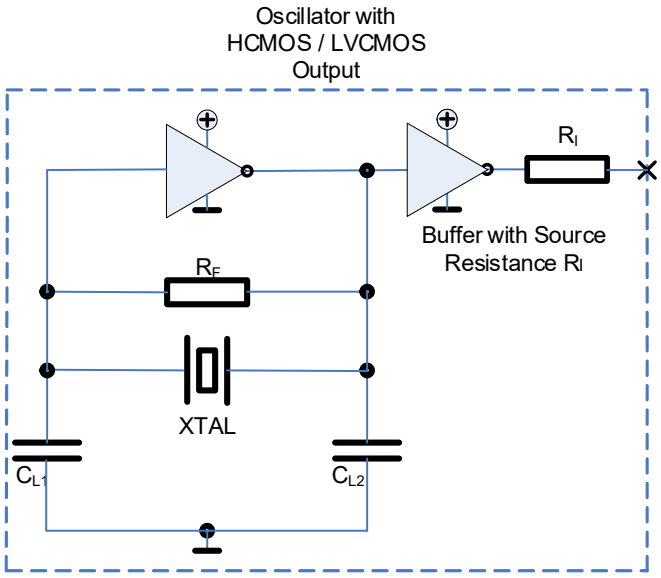
Recommendations for source impedance termination using HCMOS XOs

Most of the oscillators in the frequency range below 150 MHz offer a single ended HCMOS or LVCMOS compatible output with a rail-to-rail output swing. The acronym CMOS comes from the Complementary Metal Oxide Semiconductor, which means that the output buffer of the oscillator is built from complementary p-channel and n-channel MOS transistors.
Ideally, the output buffer of an oscillator can be seen as an output stage that can swing rail-to-rail. However, a practical output stage built from the MOS transistors will show some losses, which are represented by a source resistor R_I with a low impedance.



The problem:
Whenever an HCMOS output buffer with a lower source impedance is used to drive a load with a higher impedance over a PCB clock trace, an impedance mismatch occurs. Depending on the application and the PCB layout this impedance mismatch causes voltage reflections to occur from the load, which potentially create steps or glitches in the clock waveform, ringing as well as overshoots and undershoots. Such kind of degraded waveforms can result in poor system performance by degrading the clock signal at the receiver end, causing false clocking of data and generating unwanted triggering.

The reason for termination:
The output of the oscillator will typically feed a trace on the PCB, which can only be seen as a simple connection if it is sufficiently short. However, longer clock traces on a PCB can no longer be simplified as a lumped trace. Effectively, a longer clock trace on the PCB must be considered as a transmission line, which means that clock signal edges travel along the PCB trace at a fast propagation speed.
If the length of PCB trace exceeds certain limits, a matching of the transmission line impedance is required. Depending on the signal standard, the impedance matching is done at the receiver side, the transmitter side or even on both sides. Typically, termination resistors are used for impedance matching. Preferably, impedance matching is done at both ends of the transmission line, to avoid reflections at both sides. However, in HCMOS circuits a termination at the receiver side is not allowed.

HCMOS termination:
Typically, an HCMOS compatible input of a receiver shows a high input resistance in parallel with a small pin input capacitance. Termination resistors aren't acceptable at the receiver side, as a HCMOS receiver input requires a rail-to-rail swing to detect "H" and "L" levels properly. Adding a termination resistor at the receiver end of the transmission line would reduce the clock signal swing, and the input signal to the receiver would probably no longer meet the required threshold levels. However, a quasi-open end of a transmission line at the receiver side will cause signal reflections that travel back to the transmitter, i.e. to the buffer output stage of the oscillator. That is why an impedance matching at the transmitter side (i.e. the output of the oscillator) is recommended, to avoid further reflections of pulses that were already reflected at the receiver side. By this termination method, the waveform will not be degenerated, and will meet the standard waveform required by HCMOS receivers

Clock pulses and their spectral content:
First of all, it's important to understand that the need for impedance matching does not depend on the clock frequency itself, but on the rise and fall time of the signal edges that travel along the PCB trace. In fact, very fast rising and falling edges will cause a high frequency spectral content at multiples of the oscillators clock frequency. Such kind of high frequency spectral content is caused by higher order harmonics, which are contained in the almost rectangular waveform of the clock output signal.

The so-called pulse reflections will occur, if the length of the signal trace comes close to the wavelength λ of the highest frequencies inside the spectral content of the clock signal.
As the high frequency spectral content depends on the rise and fall time of the clock signal, the critical length of a PCB trace can be estimated based on the specified rise and fall times of the oscillator clock output.

The critical wavelength λ:
As a rule of thumb we can say that the critical length of a signal trace should be 6 times shorter than the wavelength λ of the harmonic components that dominate the duration of a rising or falling edge of the clock signal.
To calculate the wavelength λ, we have to take the propagation speed of a signal edge on the transmission line into account.

The propagation speed along the transmission line is determined by the PCB base material. For FR4 PCB material with an $\varepsilon = 4$ the propagation speed V_{Sig} can be estimated as follows:

$$V_{sig} = \frac{c}{\sqrt{\varepsilon}} \text{ and } \varepsilon = 4 \text{ for FR4 PCB material, and } c = 300.000\ \frac{km}{s}$$

$$V_{sig} = \frac{300.000\ \left[\frac{km}{s}\right]}{\sqrt{4}} = 150.000\ \left[\frac{km}{s}\right] = 150\ \left[\frac{mm}{ns}\right] = 15\ \left[\frac{cm}{ns}\right]$$

It means that a signal edge travels on a PCB trace with a speed of 15cm per nanosecond. We can also say that the pulse travels a distance of 1 km in a time as short as 6.7µs. Thinking in PCB dimensions, the propagation speed of the clock signal edges is 67 ps per cm [0.067 ns/cm].

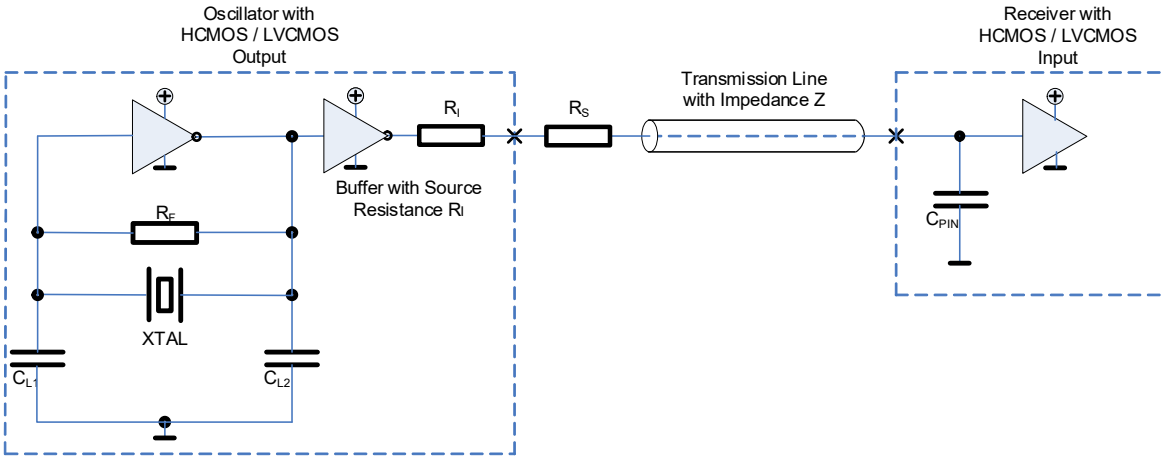
Consequences for PCB design:
Based on the assumption that a signal trace can be seen as a lumped trace if its length is shorter than 1/6th of the wavelength of a fast pulse travelling on that trace, we can estimate the critical length of a trace versus the rise & fall time of a clock signal, if the rise and fall time is given at 10% ~ 90% of the voltage swing. If the rise and fall time is specified at 20% and 80% of the voltage swing, a calculation based on 1/4th of the wavelength is acceptable.

actual / measured rise & fall time*	speed on PCB trace	wavelength of pulse on PCB trace	trace requires a termination, if longer than 1/6th of wavelength
[ns]	[cm/ns]	[cm]	[cm]
5	15	75	12.5
4	15	60	10
3	15	45	7.5
2	15	30	5
1	15	15	2.5
0.5	15	7.5	1.25

*Note that specified maximum rise & fall time in XO datasheets may be different from actually measured rise & fall time.

The source impedance termination:

As a termination at the receiver end is not allowed, an impedance matching between the oscillators output and the transmission line is recommended to avoid reflections to travel in both directions of the PCB trace. Assuming that the output of the oscillator has a source impedance R_I, and the transmission line has a characteristic impedance Z that is higher than the R_I, a series resistor R_S should be added. For best impedance matching, the sum of R_I and R_S should be equal to the characteristic impedance Z. The best value of R_S might be determined experimentally, especially if the impedance Z of the PCB trace is unknown.



Summary:

If using clock oscillators with a HCMOS output, a series resistor R_S should be placed very close to the output of the oscillator. The sum of the source impedance R_I and the series resistor R_S should be equal to the impedance Z of the transmission line. The purpose of this recommended configuration is to avoid a further reflection of pulses that are reflected at the receiver end of the transmission line. Typically, termination resistors at the receiver side are not recommended, as they will reduce the voltage swing of the clock signal, and required threshold levels at the receiver side might no longer be reached.

